

MODEL NAME : *VAZA0*
PCB NO : *LA-9262P (DAB0000I010)*
BOM P/N :

Dell/Compal Confidential

Schematic Document

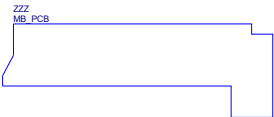
Murcielgo MLK (Haswell ULT)

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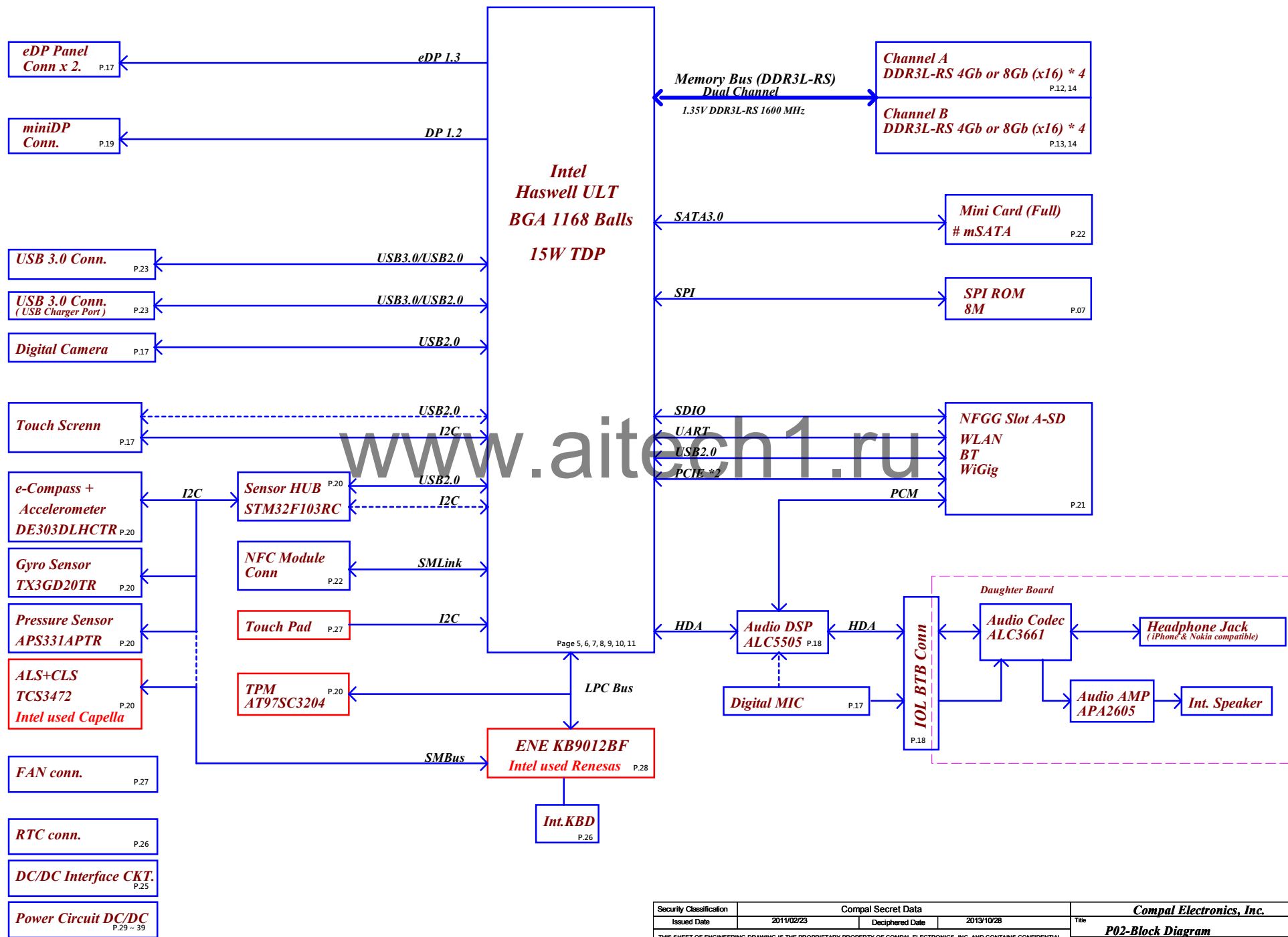
2013-04-19

Rev: 1.0

Highlight the short pad for 0 ohm

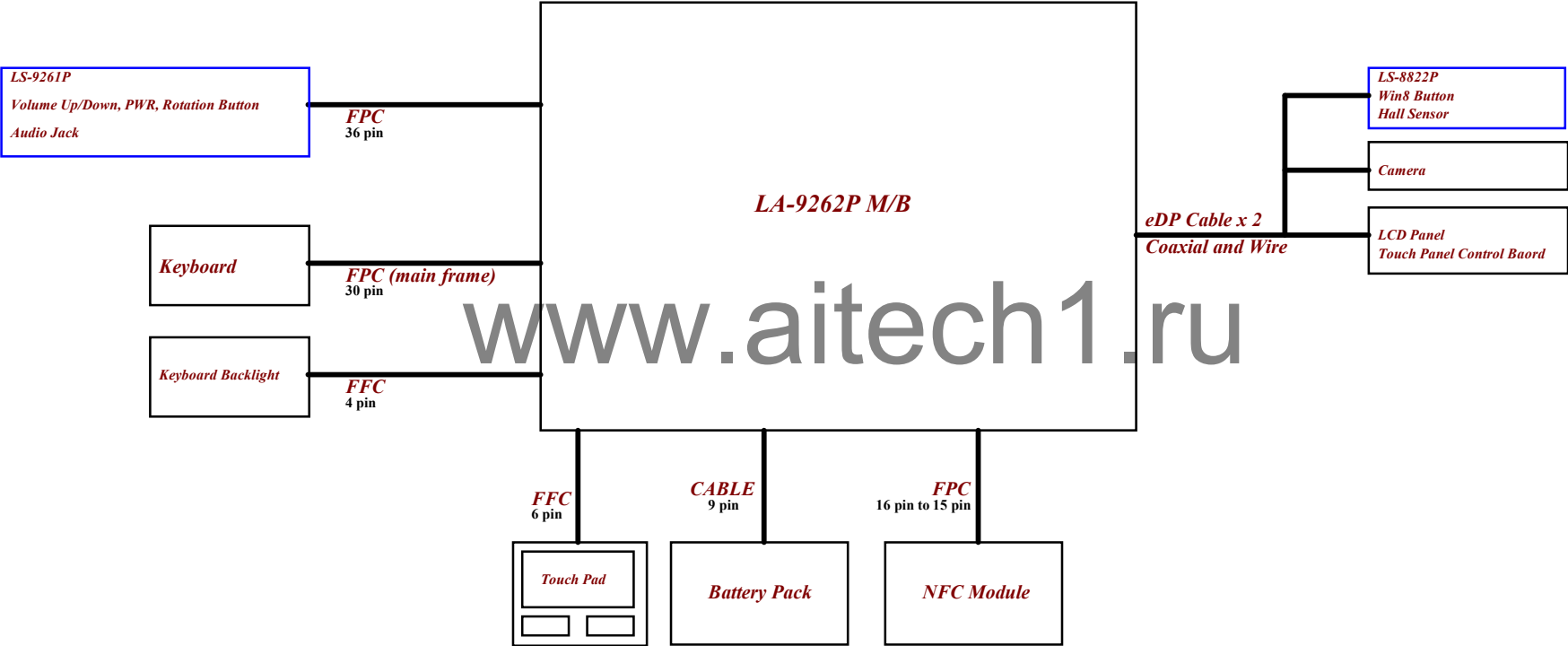


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Project Code : VAZA0
File Name : LA-9262P



Board ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra	100K +/- 1%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3
0	0				
1	12K +/- 1%				
2	15K +/- 1%				
3	20K +/- 1%				
4	27K +/- 1%				
5	33K +/- 1%				
6	43K +/- 1%				
7	56K +/- 1%				
8	75K +/- 1%				
9	100K +/- 1%				
10	130K +/- 1%				
11	160K +/- 1%				
12	200K +/- 1%				
13	240K +/- 1%				
14	270K +/- 1%				
15	330K +/- 1%				
16	430K +/- 1%				
17	560K +/- 1%				
18	750K +/- 1%				
19	NC				

BOARD ID Table

Board ID	PCB Revision
0	CS 0.1
1	CS 0.2
2	CS 0.3
3	CS 0.4
4	CS 0.5
5	CS 1.0
6	
7	
8	
9	
10	Non-CS 0.1
11	Non-CS 0.2
12	Non-CS 0.3
13	Non-CS 0.4
14	Non-CS 1.0
15	
16	
17	
18	
19	

PCH USB Port Mapping	USB PORT#	DESTINATION
	0	External USB3
	1	External USB3
	2	NGFF CARD WLAN
	3	Touch Panel
	4	Camera
	5	Sensors HUB
	6	
	7	

SMBUS Control Table

	SOURCE	NGFF	BATT	Charger	NFC	XDP	DDR3 SPD	ALS	Touch Pad
EC_SMB_CK1 EC_SMB_DA1	KB9012		V	V					
EC_SMB_CK2 EC_SMB_DA2	KB9012							V	
PCH_SMLCLK PCH_SMLDATA	PCH	V			V				
PCH_SML1CLK PCH_SML1DATA	PCH								
MEM_SMBCLK MEM_SMBDATA	PCH					V	V		V

Link

PCH DDI Port Mapping	DDI PORT#	DESTINATION
	B	mini-DP
	C	

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0		CLKOUT_LPC_0	EC LPC
	CLKOUT_PCIE1		CLKOUT_LPC_1	TPM
	CLKOUT_PCIE2			
	CLKOUT_PCIE3	NGFF CARD WLAN		
	CLKOUT_PCIE4			
	CLKOUT_PCIE5			

SATA	DESTINATION
SATA0	m-SATA
SATA1	
SATA2	
SATA3	

PCI EXPRESS	DESTINATION
Lane 1	
Lane 2	
Lane 3	NGFF CARD WLAN
Lane 4	NGFF CARD WLAN
Lane 5	
Lane 6	

Symbol Note :

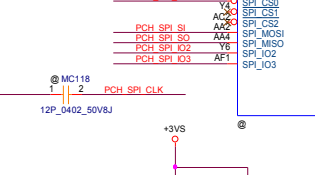
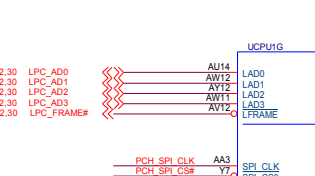
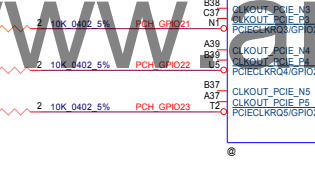
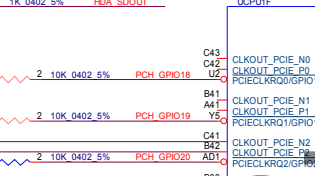
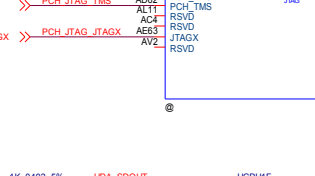
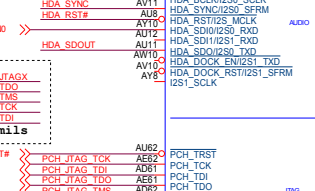
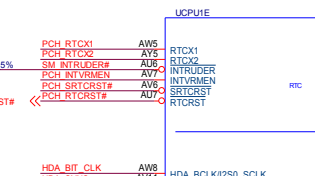
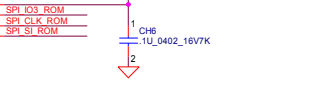
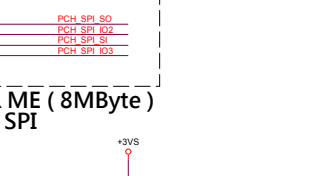
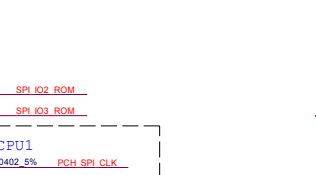
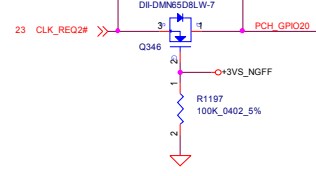
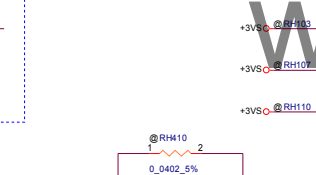
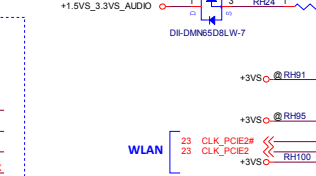
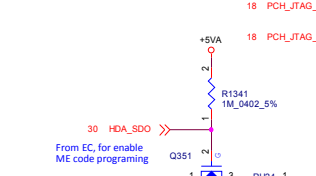
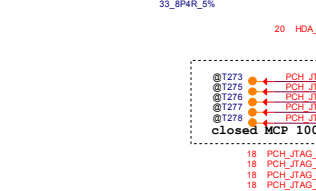
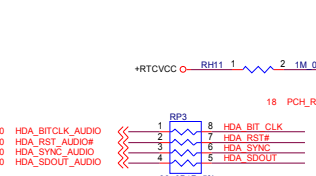
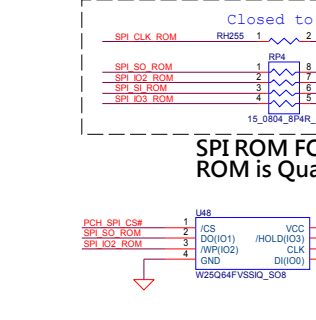
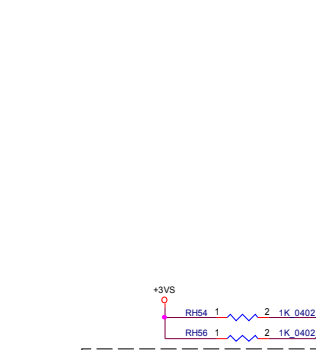
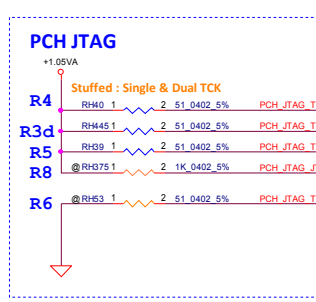
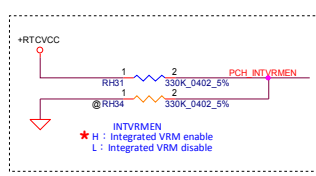
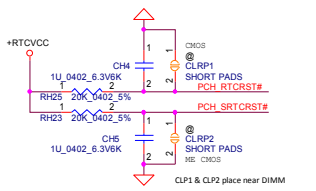
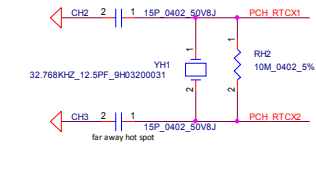


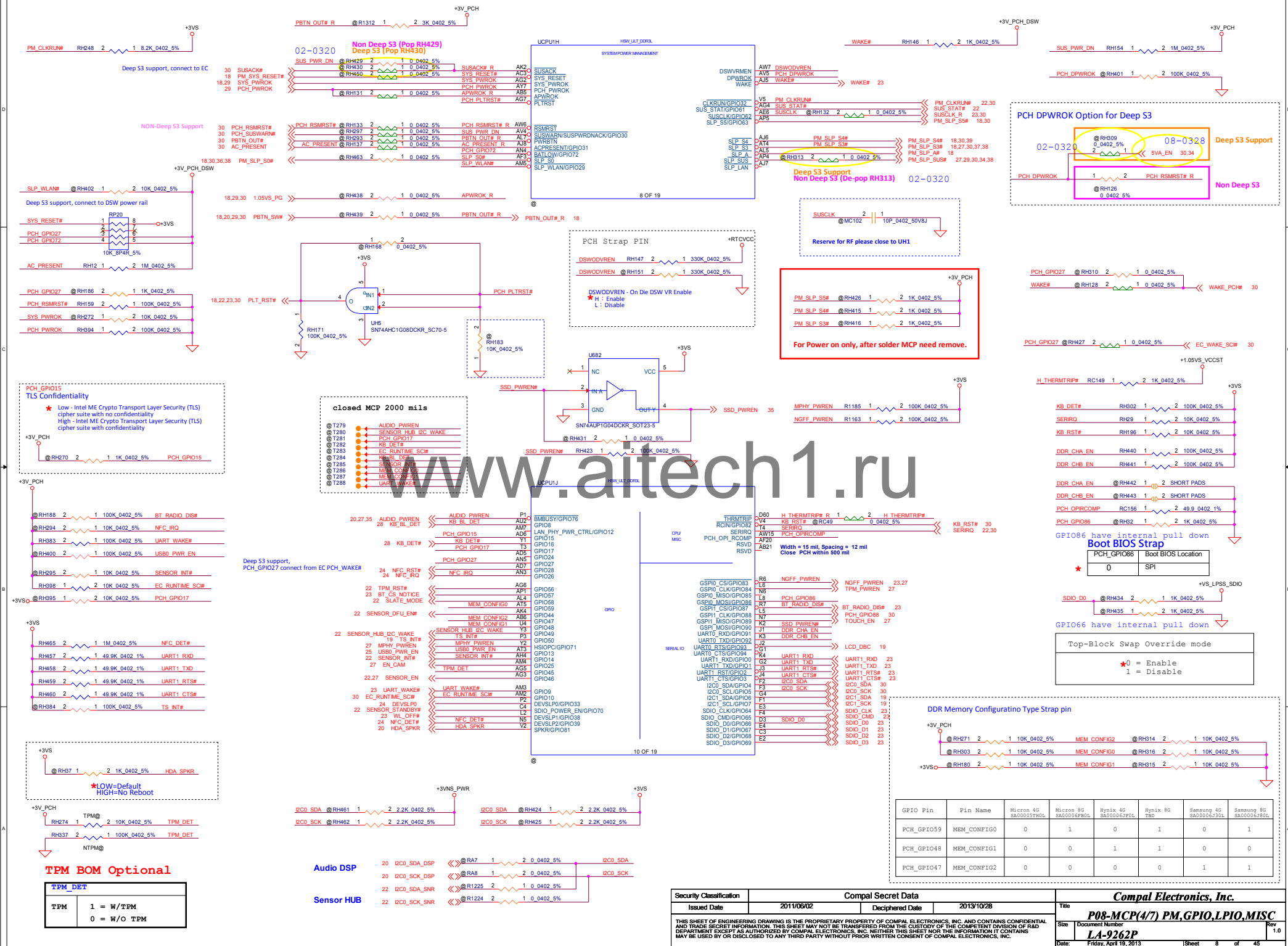
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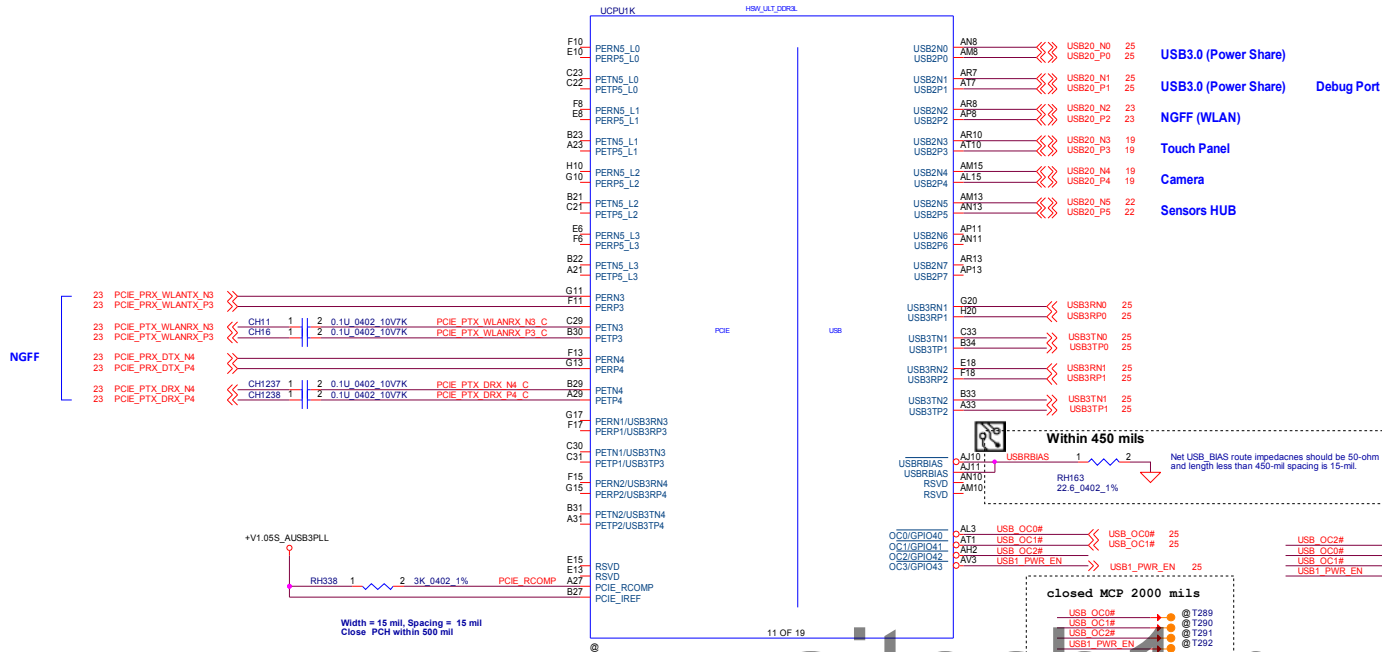


: means Analog Ground

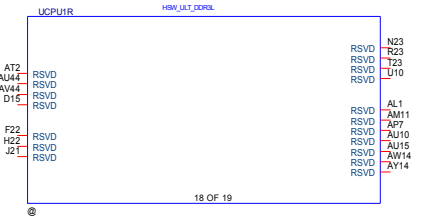
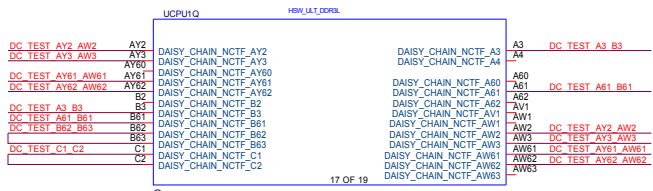
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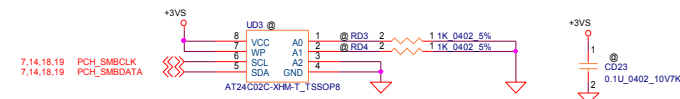
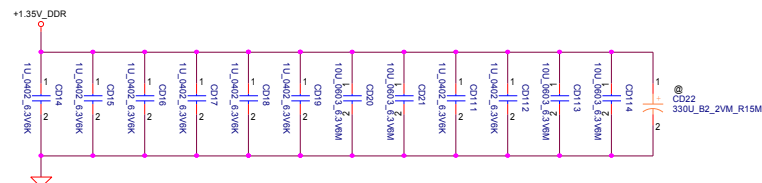
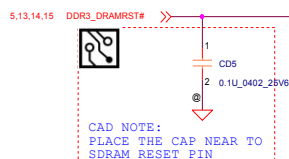
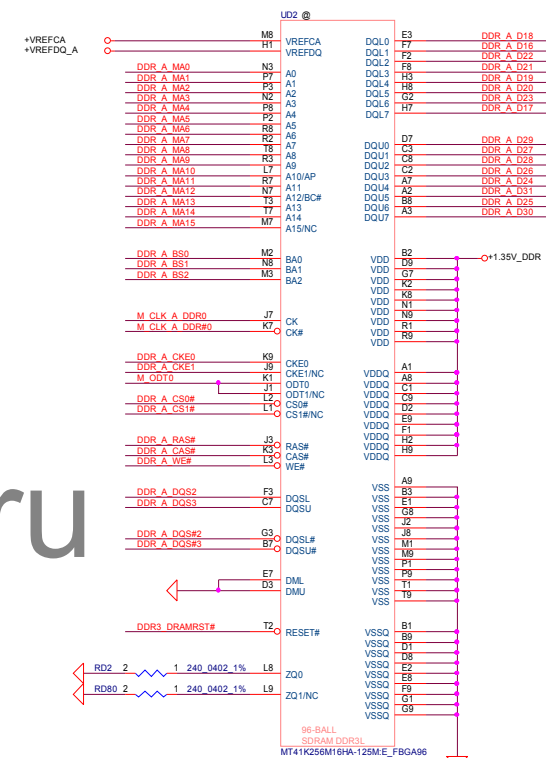




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6,13	DDR_A_DQS#[0..7]	《》	
6,13	DDR_A_DQS[0..7]	《》	
6,13	DDR_A_D[0..63]	《》	
6,13,16	DDR_A_MA[0..15]	《》	



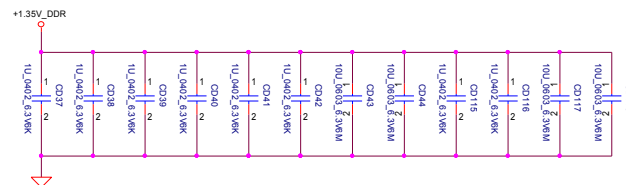
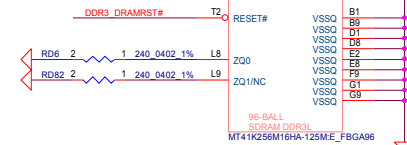
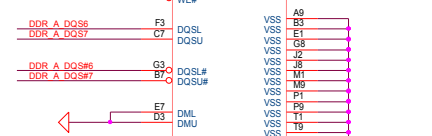
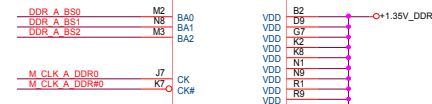
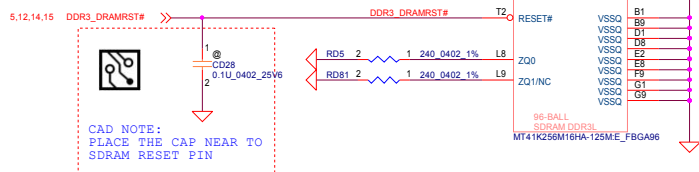
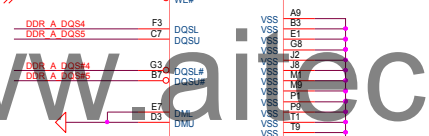
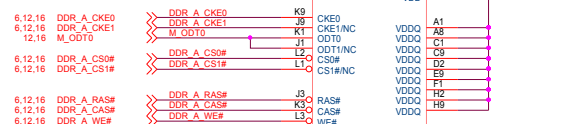
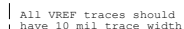
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follow INTEL PDG

CD24 2 | 1 .047U .0402 16V7K
CD25 2 | 1 .047U .0402 16V7K +VREFCA

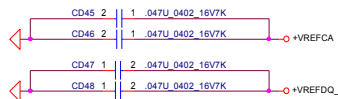
CD26 1 | 2 .047U .0402 16V7K
CD27 1 | 2 .047U .0402 16V7K +VREFDQ_A

**PLACE THESE CAPS
NEAR TO RESPECTIVE DIMM PINS**



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				Size	Document Number	Rev
					LA-9262P	1.
Date:	Friday, April 19, 2013		Sheet	13	of	45

follow INTEL PDG



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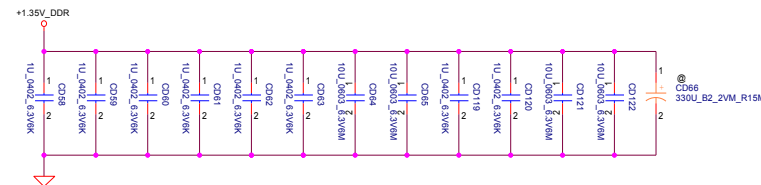
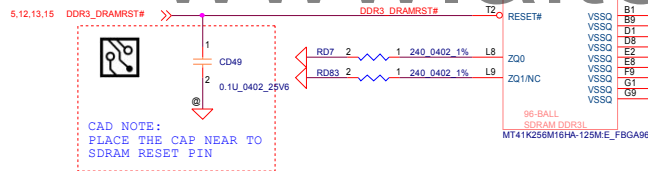


- 6.15 DDR_B_DQS#(0..7) <<>
- 6.15 DDR_B_DQS(0..7) <<>
- 6.15 DDR_B_DQ(0..63) <<>
- 6.15,16 DDR_B_MA(0..15) <<>

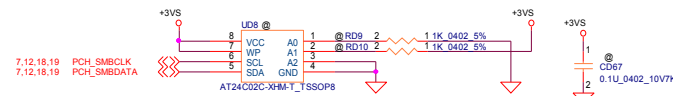
All VREF traces should
have 10 mil trace width



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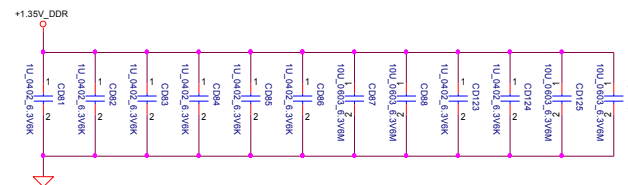
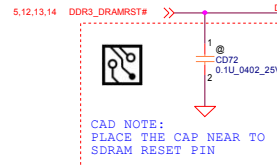
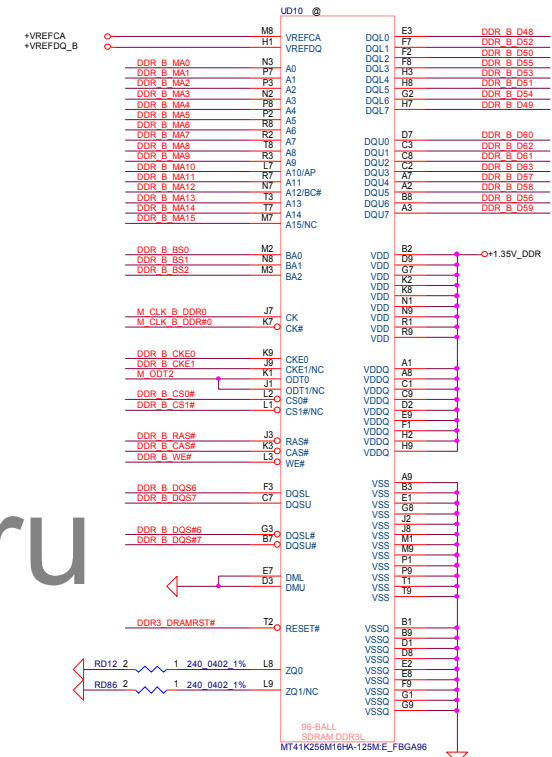
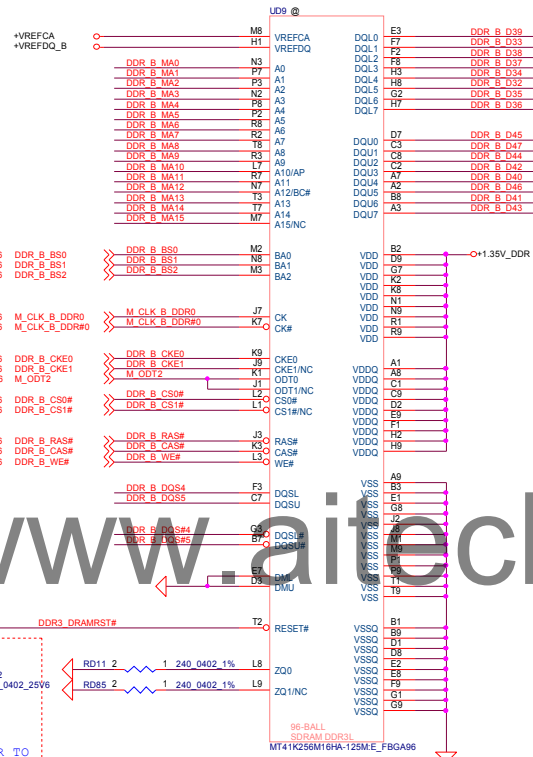
Memory Channel B SPD EEPROM



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P14-DDRIII Channel B Lower				Rev 1.0
LA-9262P				
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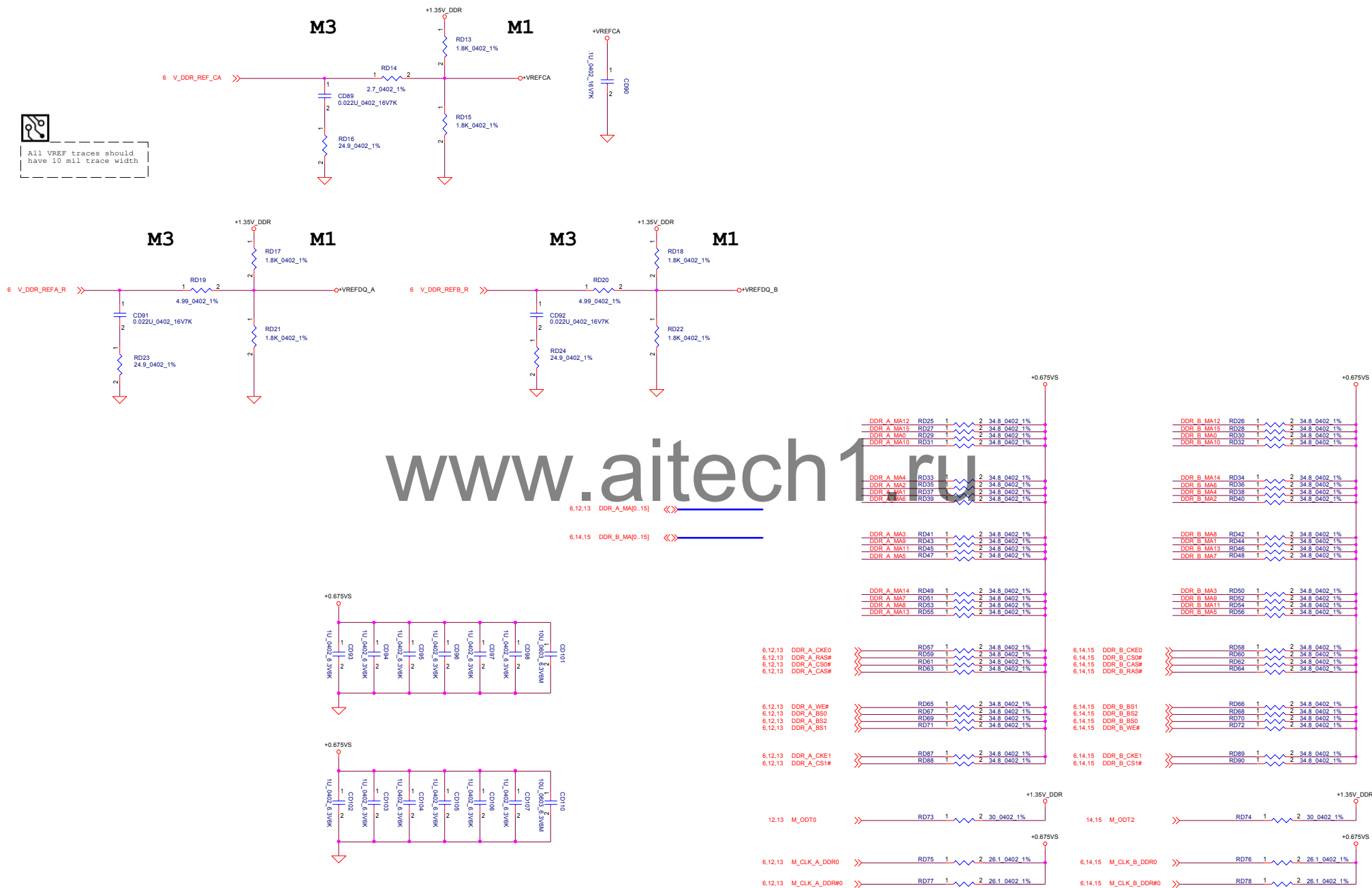
All VREF traces should have 10 mil trace width



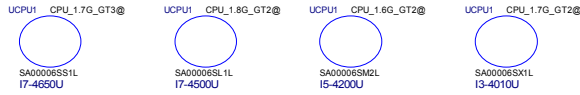
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All VREF traces should have 10 mil trace width

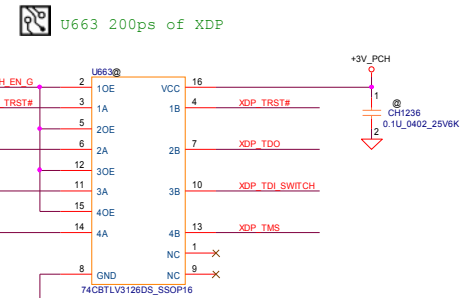
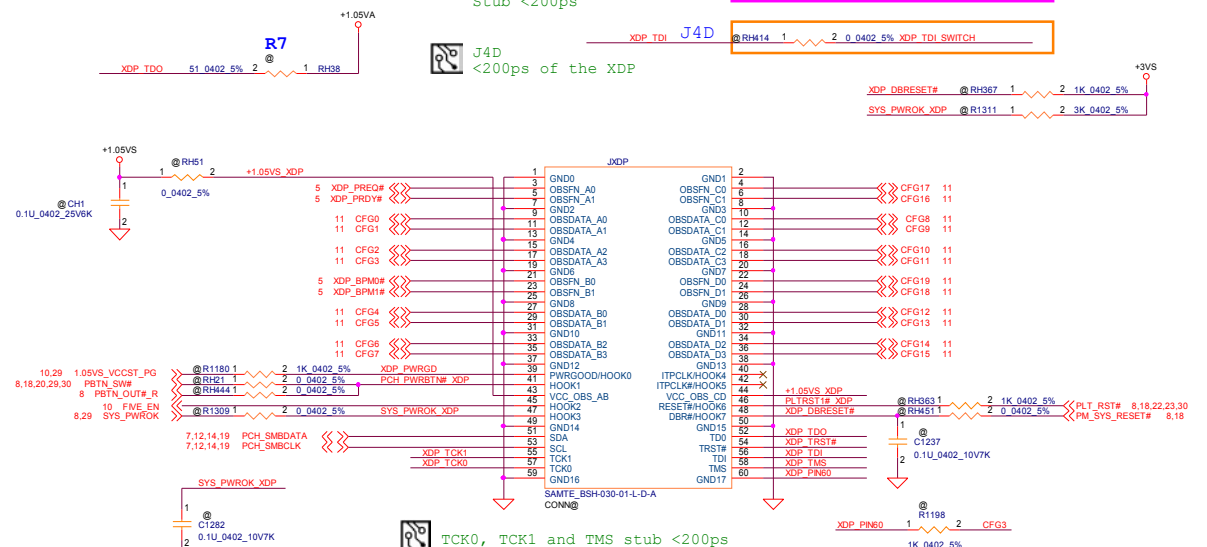


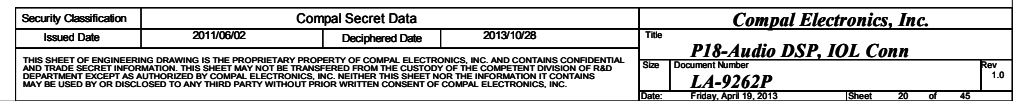
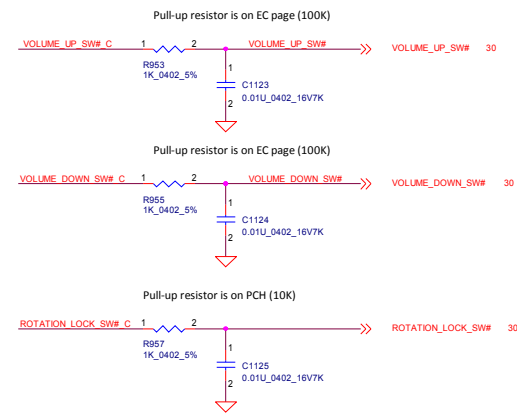
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2013/10/28		2013/10/28		LA-9262P	
2013/10/28		2013/10/28		Rev 1.0	
2013/10/28		2013/10/28		Date: Friday, April 19, 2013	
2013/10/28		2013/10/28		Sheet 16 of 45	

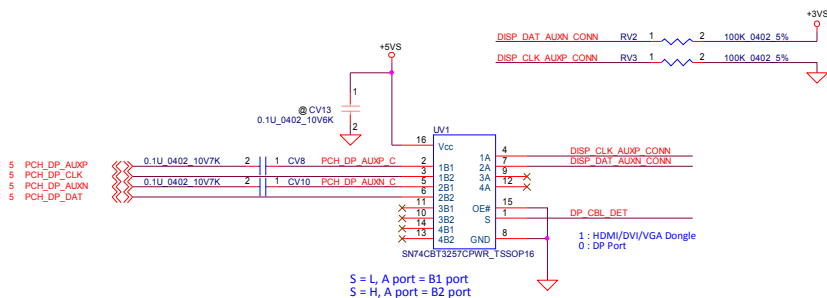


MEM_CONFIG2 MEM_CONFIG1 MEM_CONFIG0

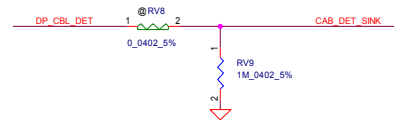
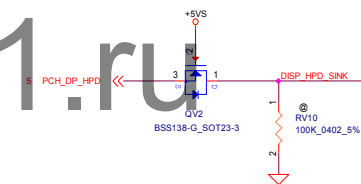
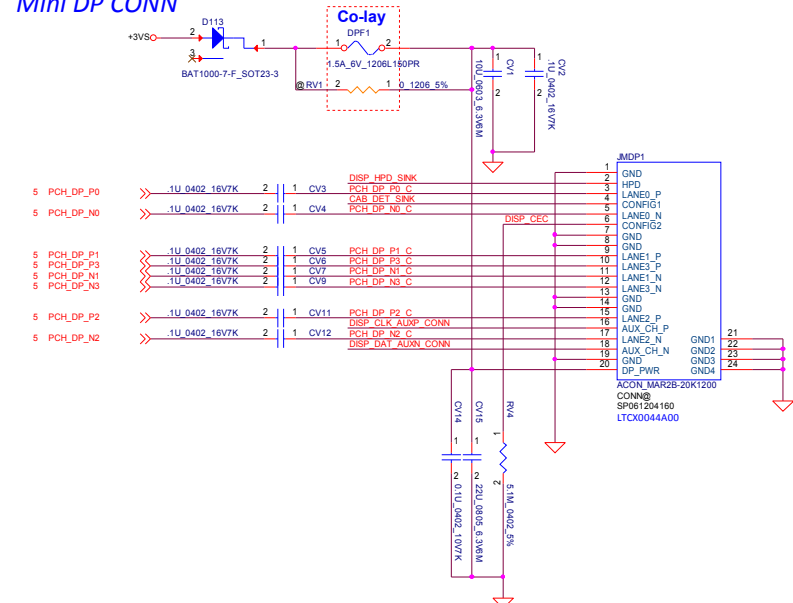


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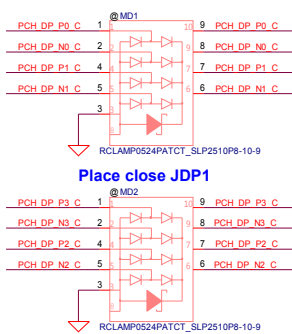




Mini DP CONN



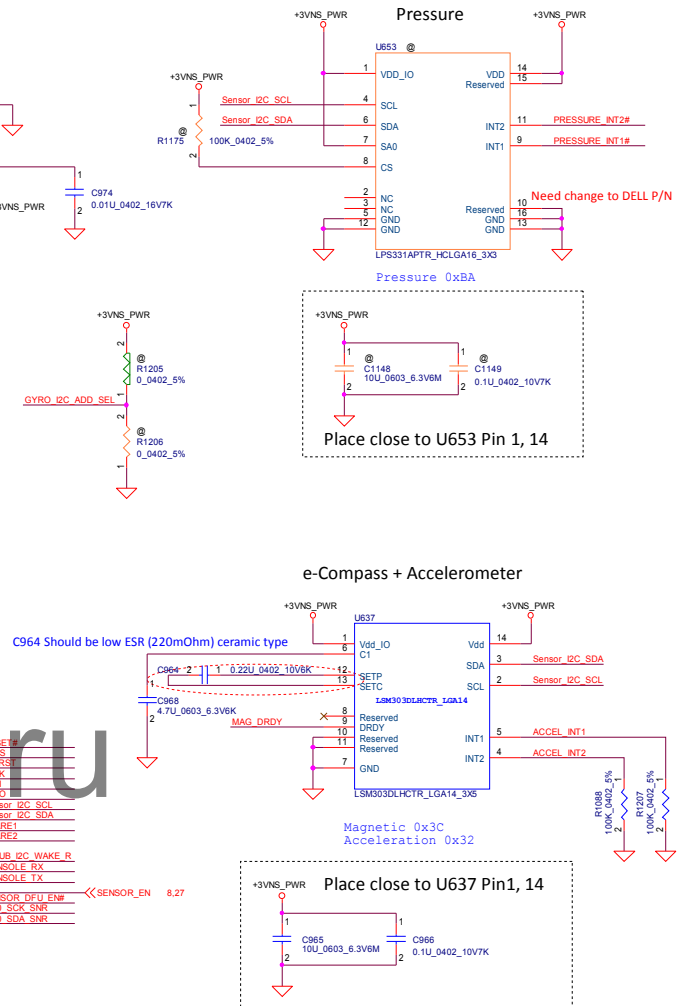
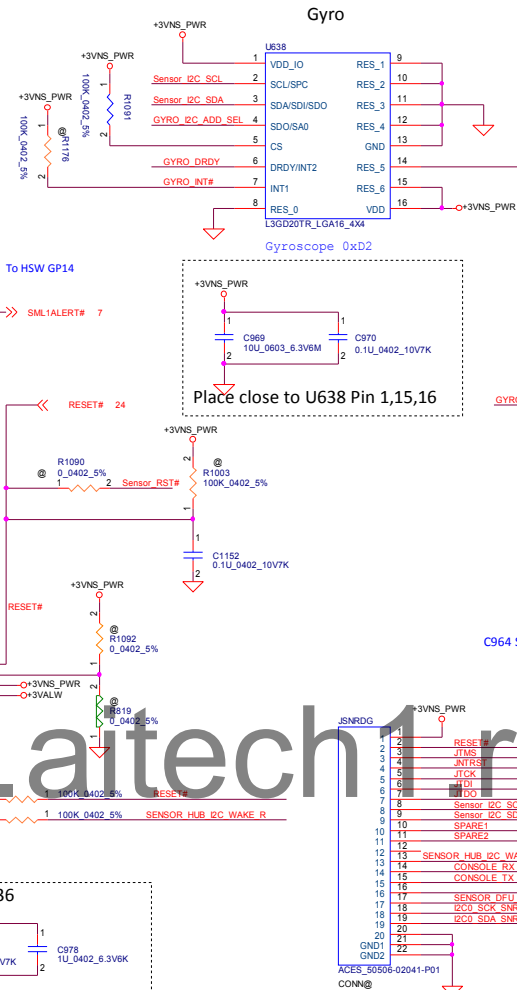
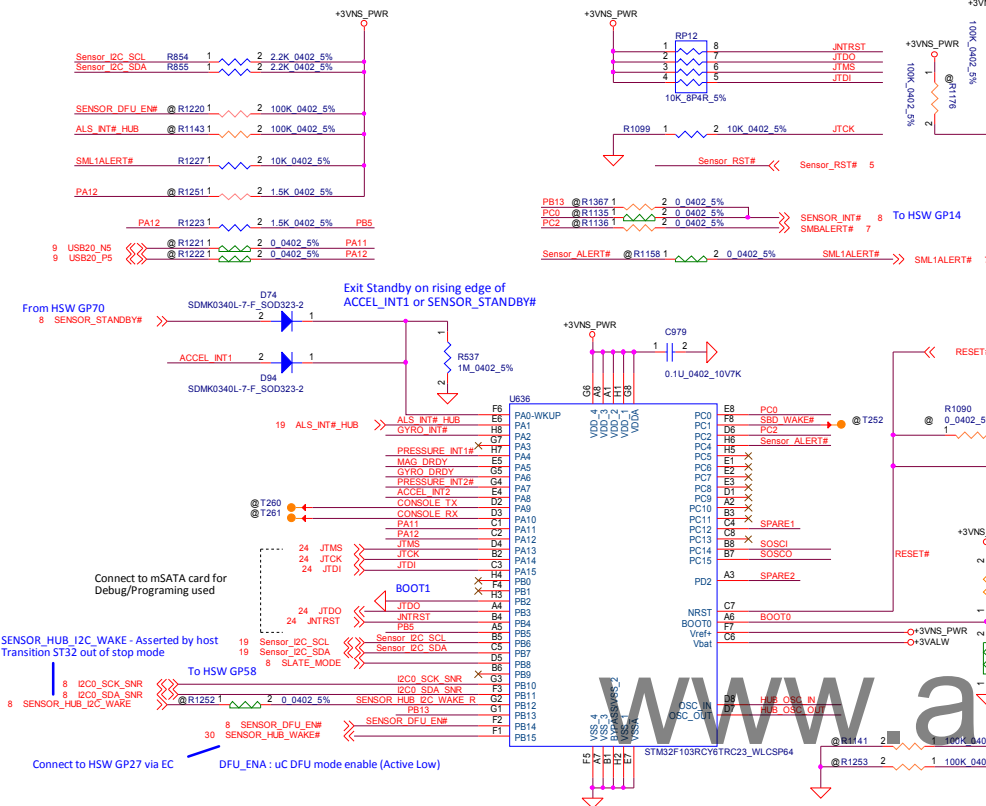
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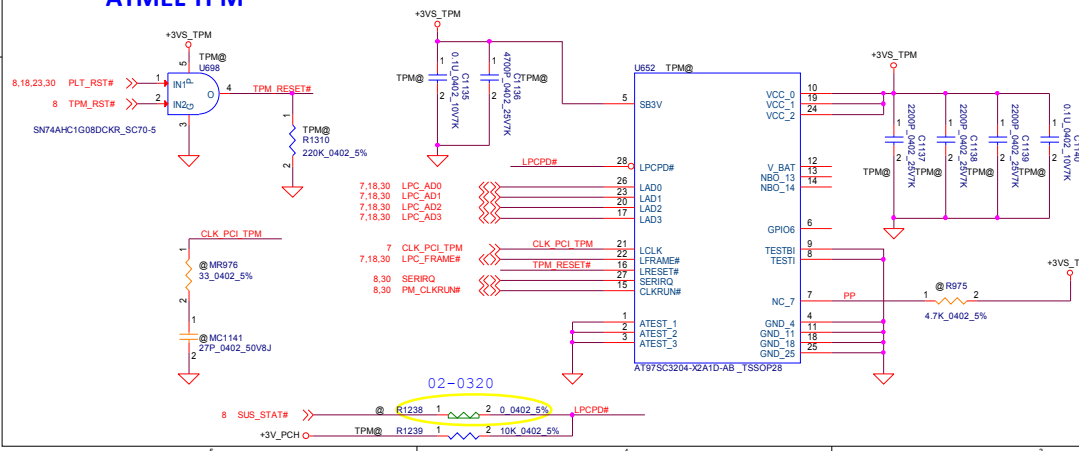
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Size	C	Document Number	LA-9262P	Rev	1.0
Date:	Friday, April 19, 2013	Sheet	21	of	45

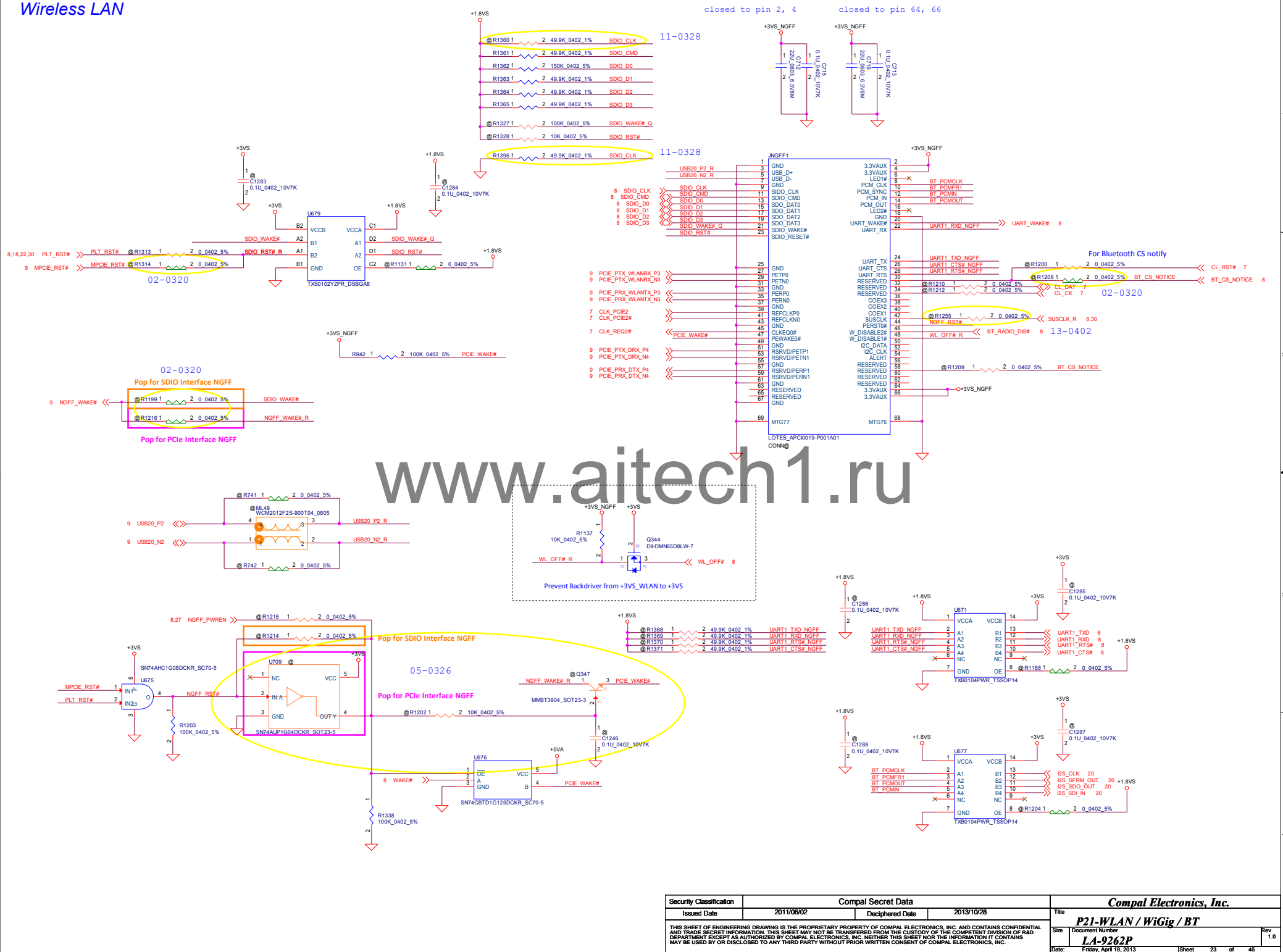
Sensor Fusion



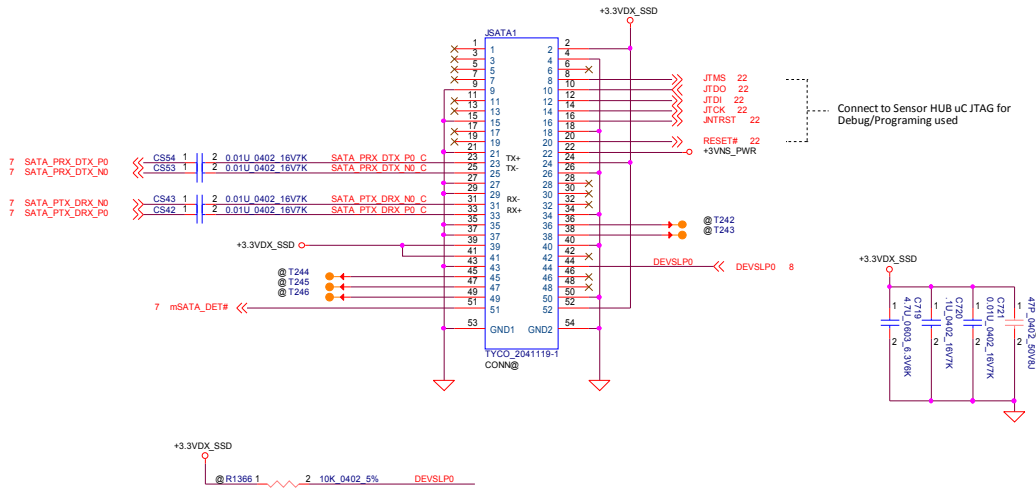
ATMEL TPM



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				Document Number LA-9262P
				Rev 1.0
Date:			Friday, April 19, 2013 Sheet 22 of 45	

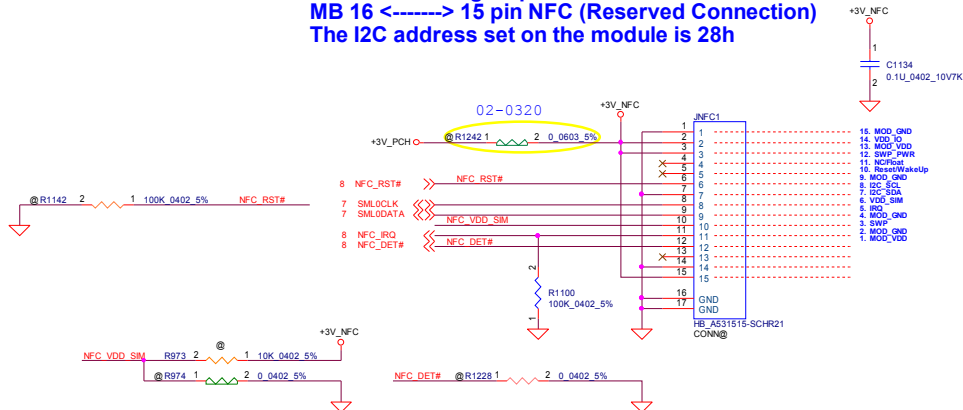


mSATA Card



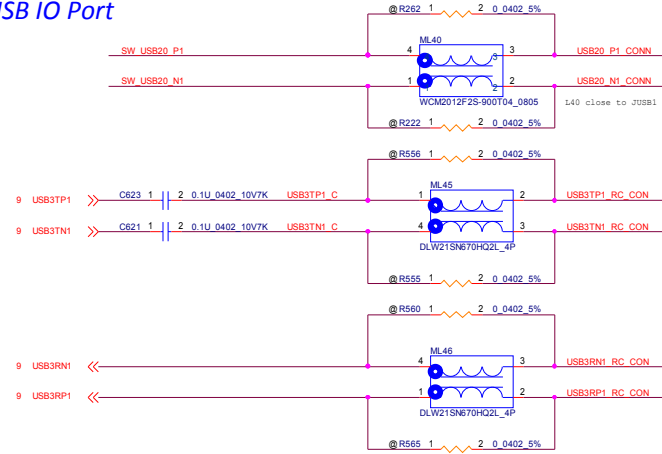
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ME Decide using 16 pin conn
MB 16 <-----> 15 pin NFC (Reserved Connection)
The I2C address set on the module is 28h

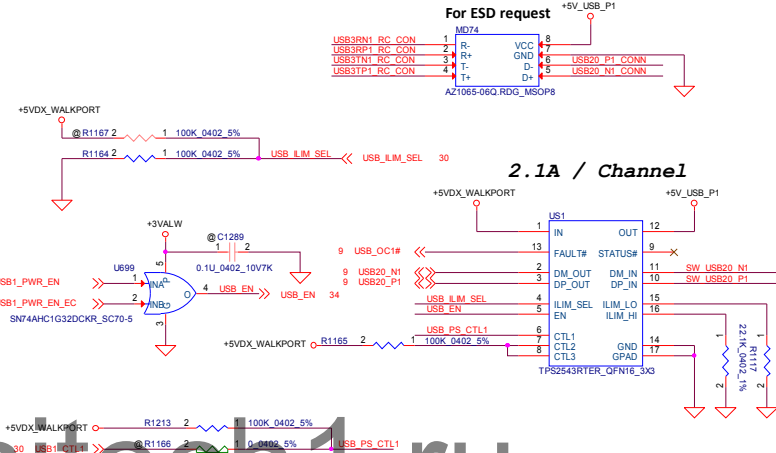
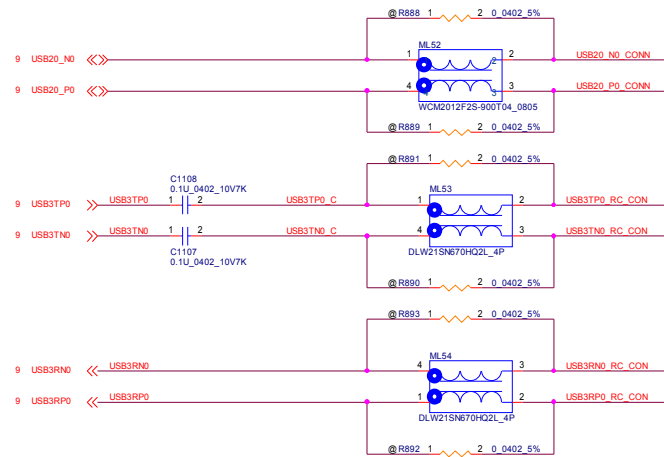


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USB IO Port



CTL1	CTL2	CTL3	ILIM_SEL	MODE
0	1	1	0	DCP_Auto
0	1	1	1	DCP_Auto
1	1	1	0	SDP
1	1	1	1	CDP



2.1A / Channel

2A / Channel

USB CONN

USB CONN

USB CONN

USB CONN

USB CONN

USB CONN

USB CONN

USB CONN

USB CONN

USB CONN

USB CONN

USB CONN

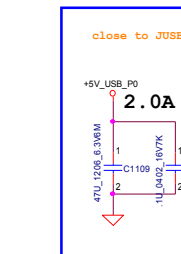
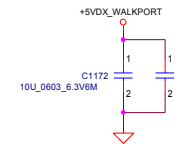
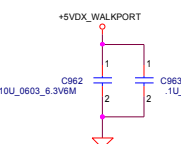
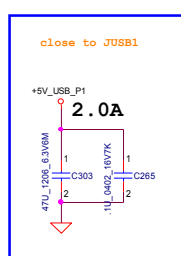
USB CONN

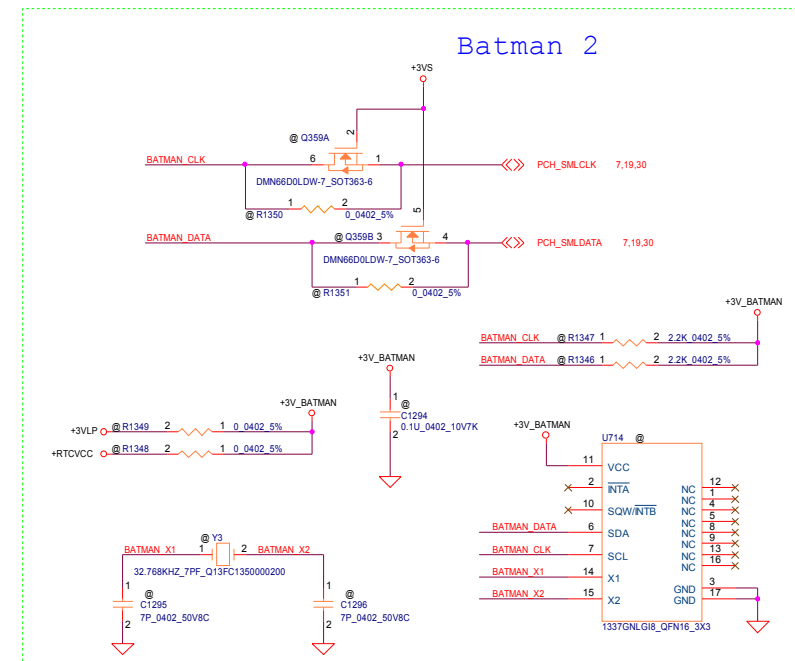
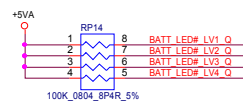
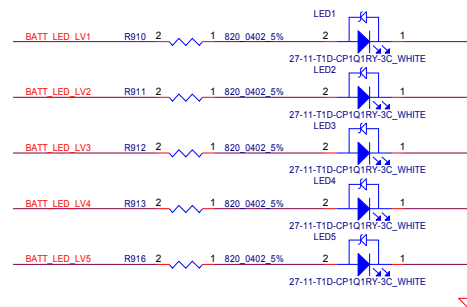
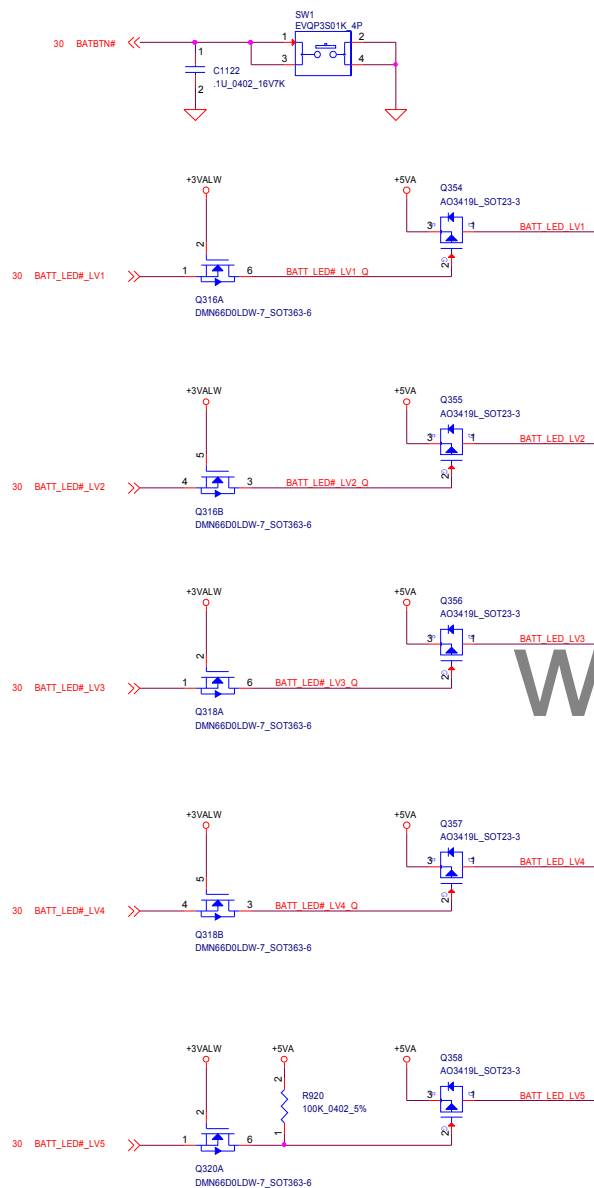
USB CONN

USB CONN

USB CONN

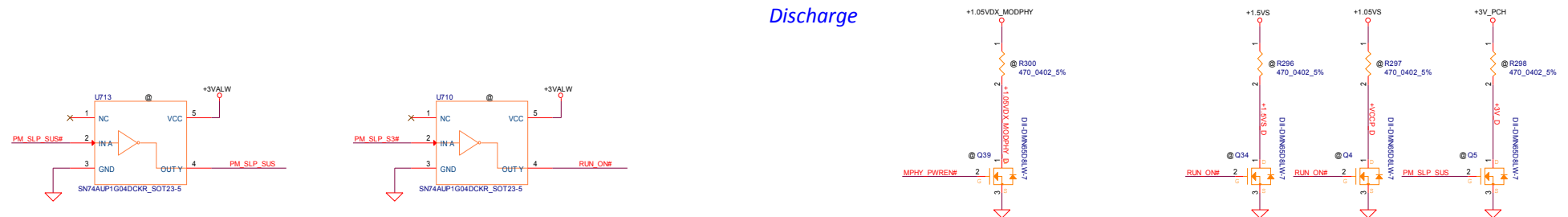
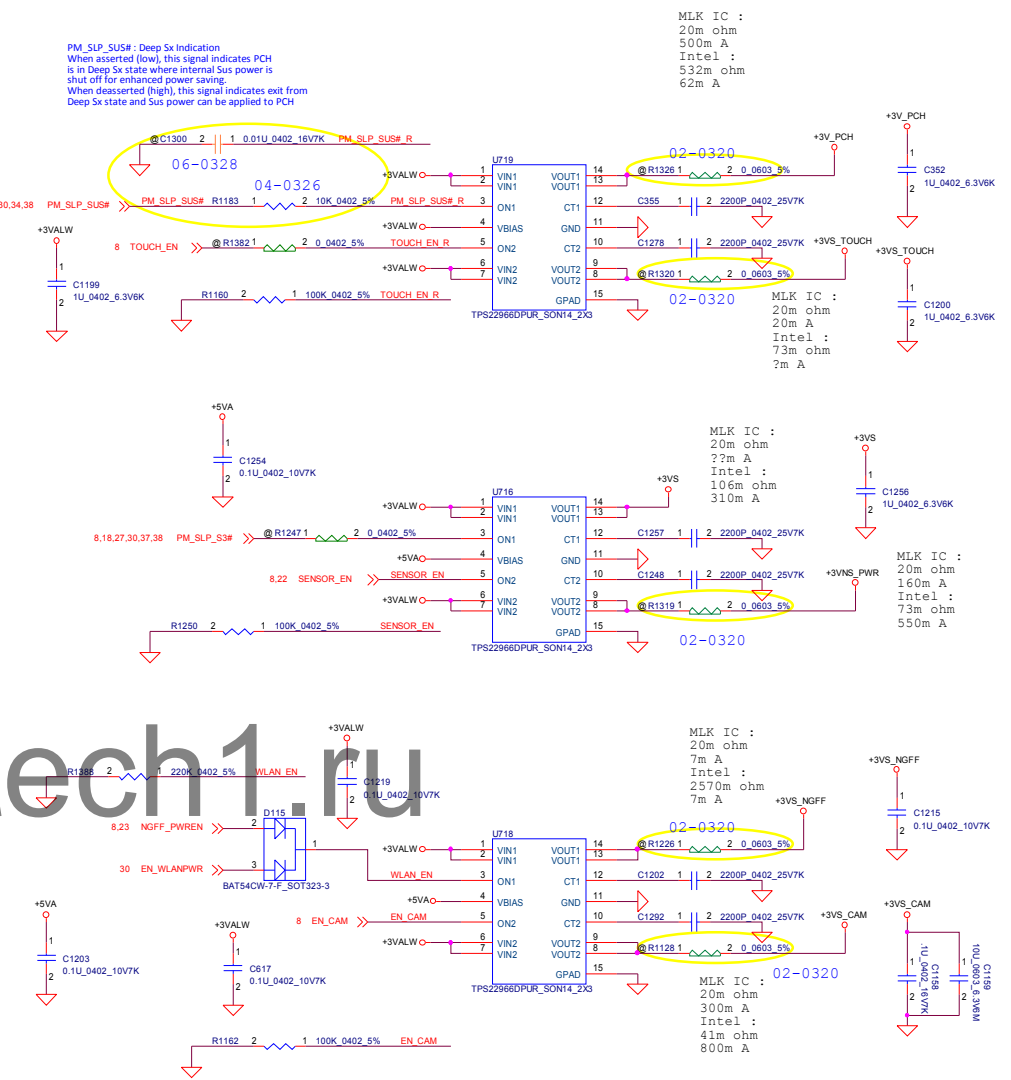
USB CONN





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2011/06/02		2013/10/28		P24-BAT LED	
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						Size	Document Number			Rev
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Diagram illustrating a 2x2 MIMO system with four antennas labeled H0, H10, H11, and H12. Each antenna is connected to an H_{3P2} CONN@ port and a ground symbol.

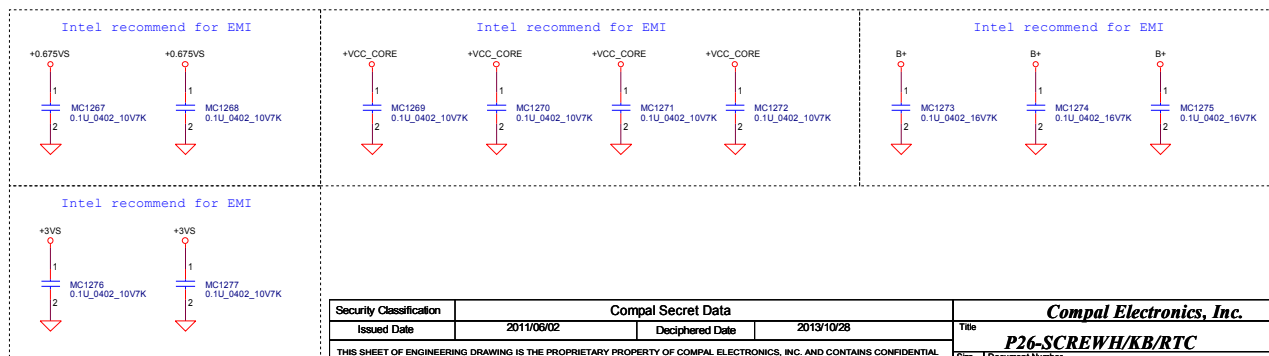
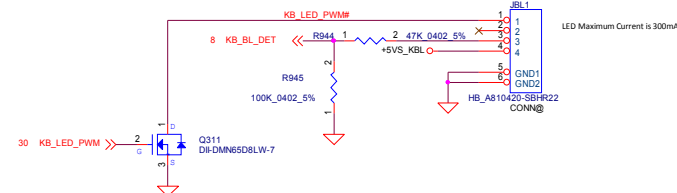
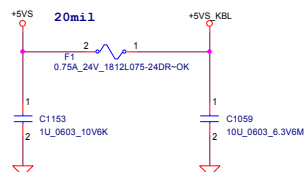
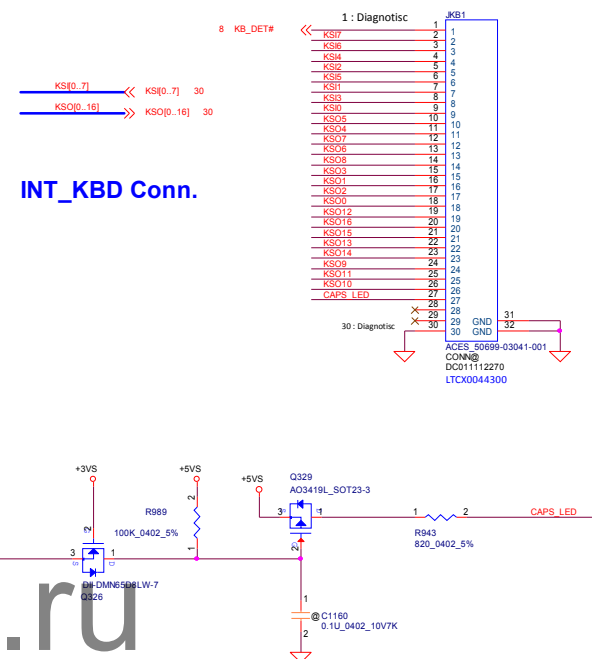
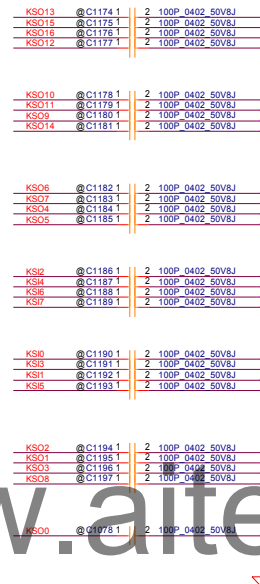
The image contains two circuit diagrams for the ACS 50271-00201-001 component.

Left Diagram:

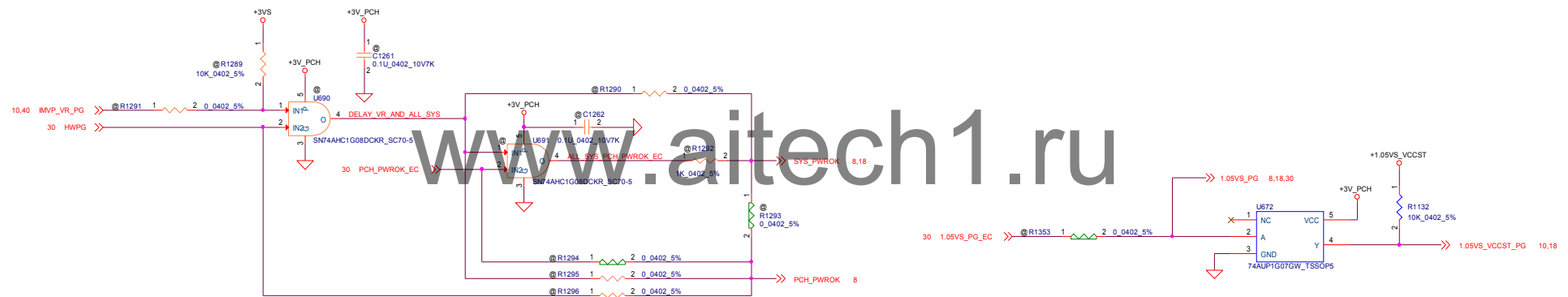
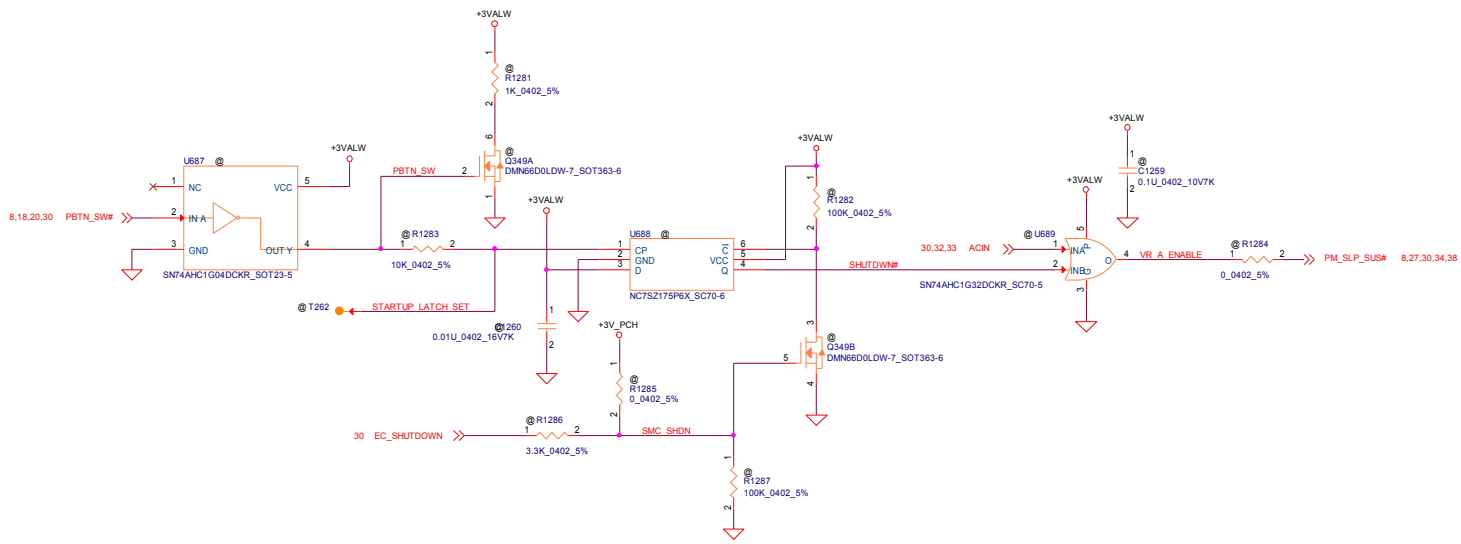
- +RTCBATT:** Connected to a 1K_0402_5% resistor.
- +3VLP:** Connected to a diode bridge circuit.
- W=20mils:** Trace width specification.
- RTCD1:** BAT54CW-7-F_SOT323-3.
- W=20mils:** Trace width specification.
- +RTCVCC:** Connected to a 12-0328 voltage divider and a 10k resistor.
- CH65:** 10uF_0402_6.3V8K capacitor.
- Ground:** Indicated by a triangle symbol.

Right Diagram:

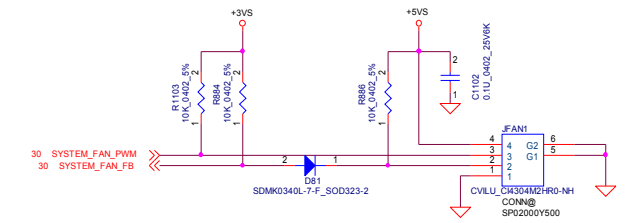
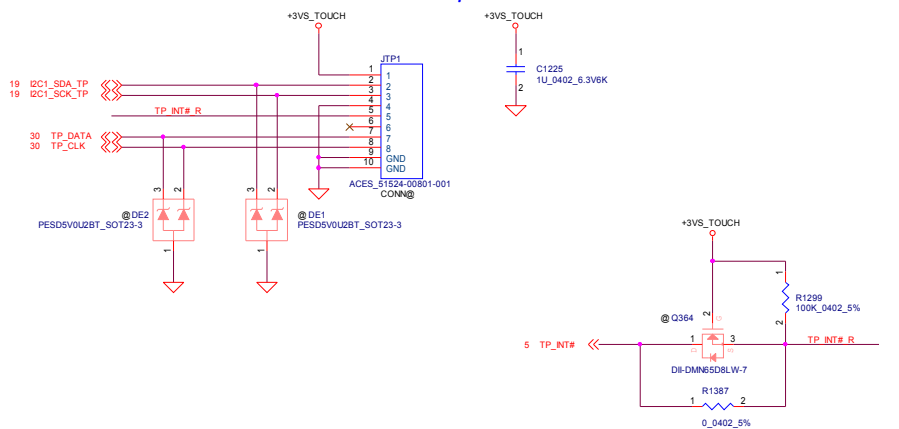
- +RTCBATT:** Connected to a 12-0328 voltage divider.
- +RTCVCC:** Connected to a 12-0328 voltage divider and a 10k resistor.
- W=20mils:** Trace width specification.
- RTCD1:** BAT54CW-7-F_SOT323-3.
- W=20mils:** Trace width specification.
- CH65:** 10uF_0402_6.3V8K capacitor.
- Ground:** Indicated by a triangle symbol.



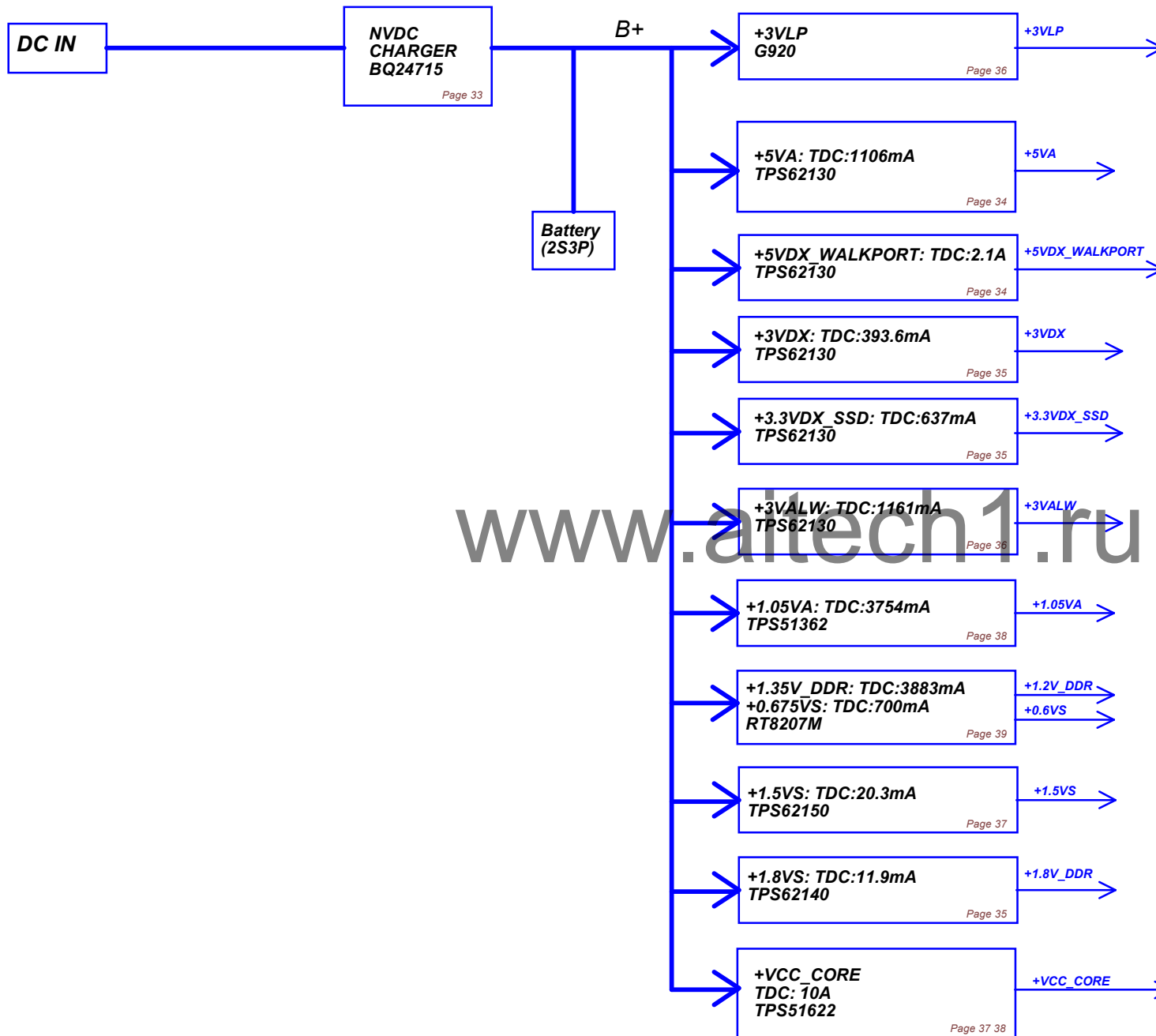
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				Size	Document Number
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Touchpad CONN

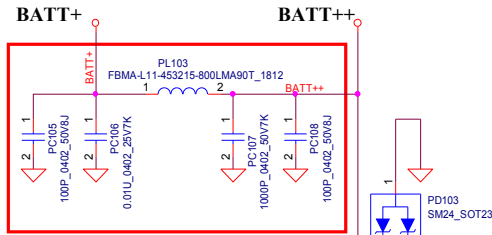
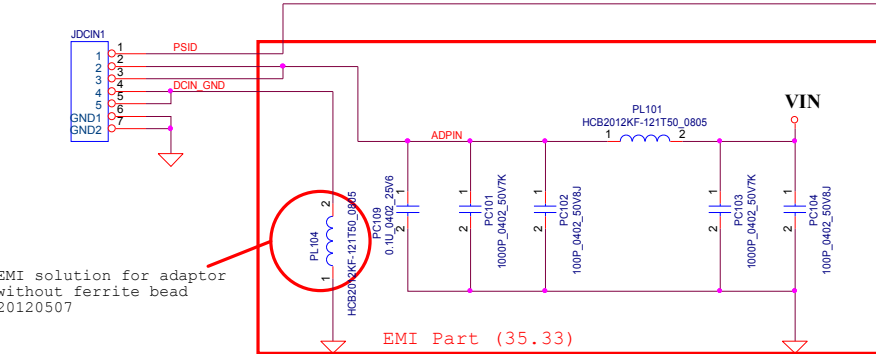


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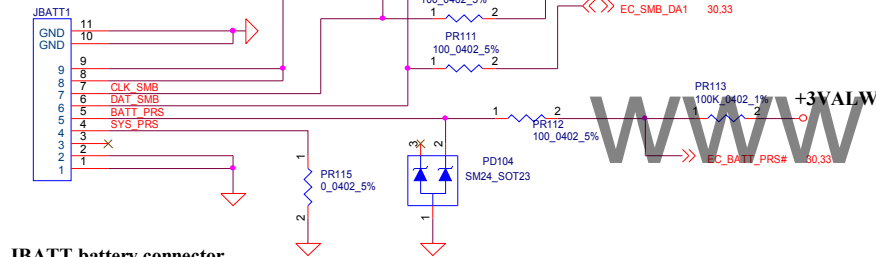


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EMI solution for adaptor without ferrite bead
20120507



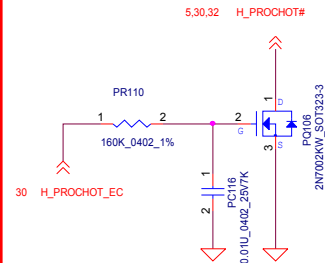
EMI Part (35.33)



JBATT battery connector

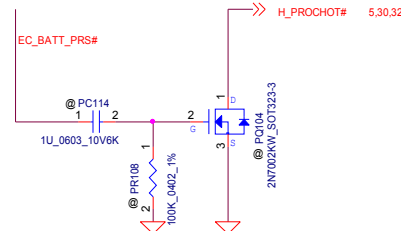
SMART Battery:
1.GND
2.GND
3.BAT_ALERT
4.SYS_PRES
5.BATT_PRS
6.DAT_SMB
7.CLK_SMB
8.BATT++
9.BATT++

Delay adaptor OC H_PROCHOT#
2ms while hybrid power transition



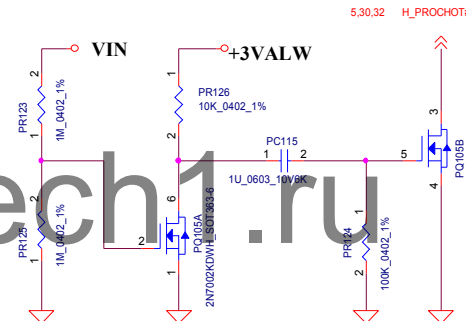
Adaptor protection:

if battery removed, adaptor only,
then trigger the H_PROCHOT#,
keep DNP in BOM since battery can not
be removed by end user



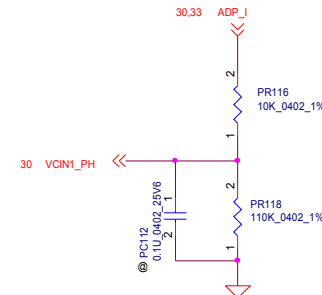
Battery protection:

asserts H_PROCHOT# when adaptor is
unplugged, keep low for 10ms
till SW_PROCHOT# is issued by EC



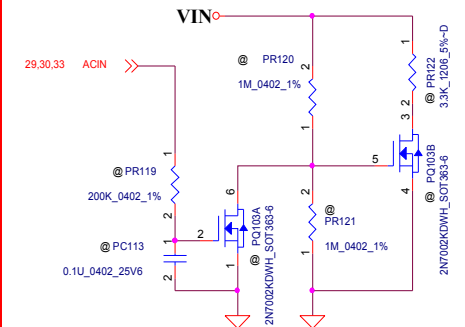
Adaptor protection:

if CP and IPCC failed, adaptor output
=rating 100% and over load 20W
then trigger the H_PROCHOT# by EC



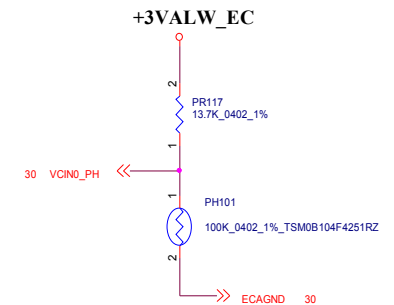
Erp lot6 Circuit

keep DNP in BOM since Dell 45W
adaptor has no hiccup mode

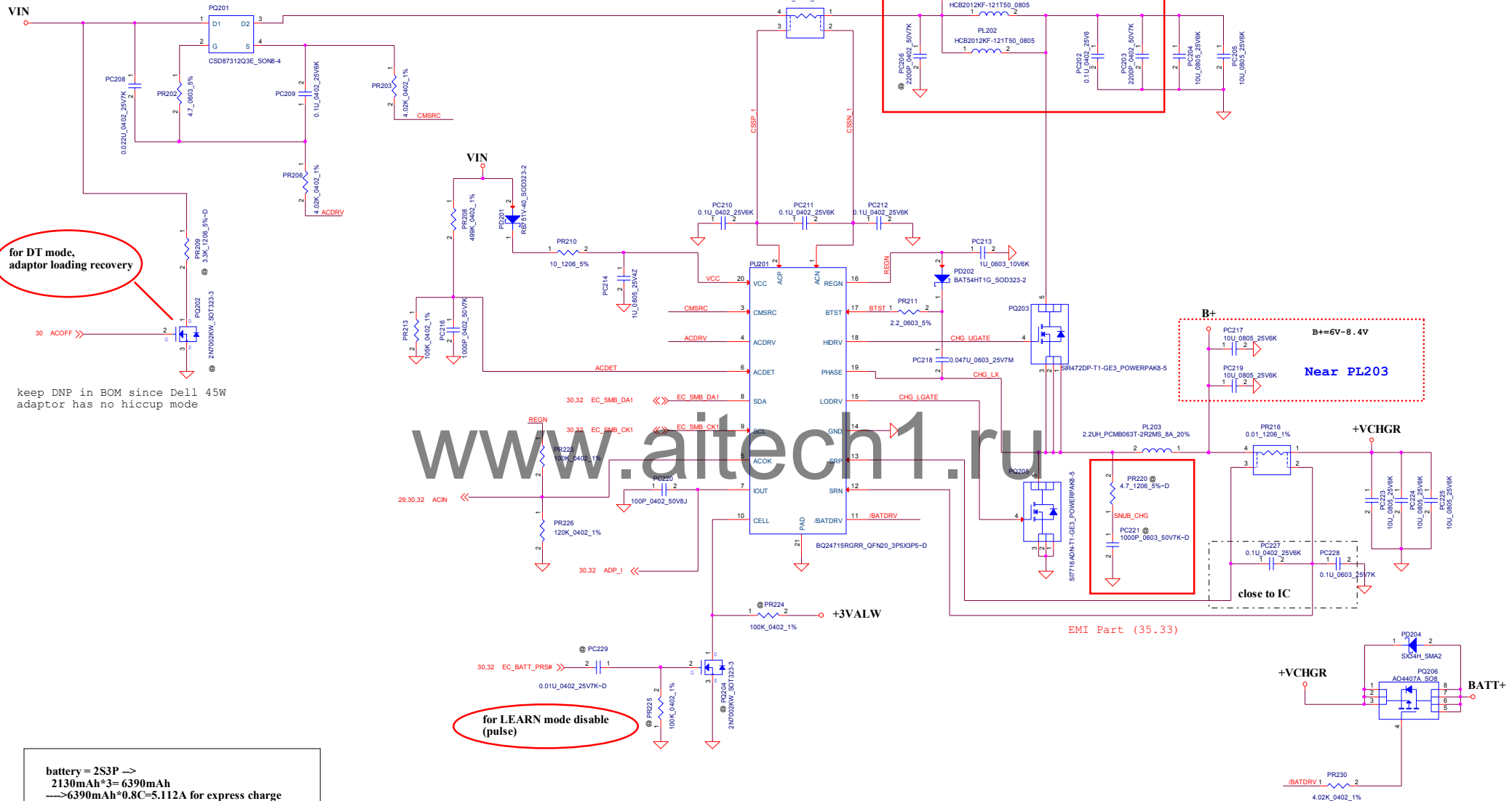


PH101 under CPU bottom side :

CPU thermal protection
@88+-3 degree C
Recovery at 80+-3 degree C

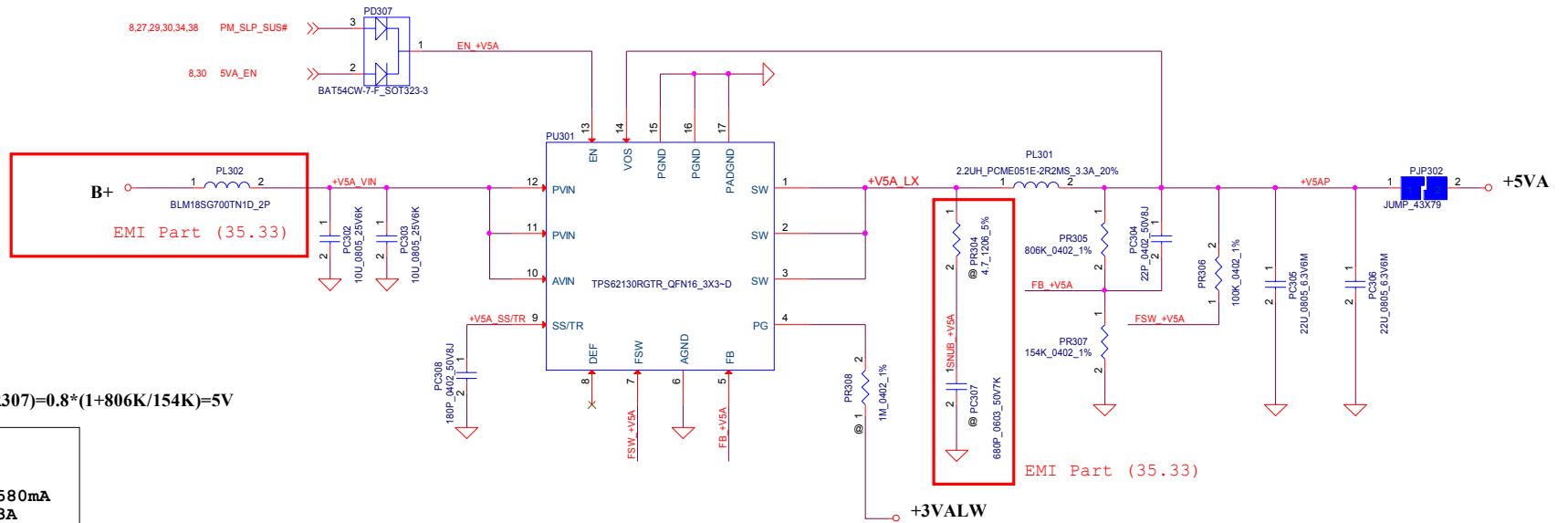


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				Sheet	32 of 45



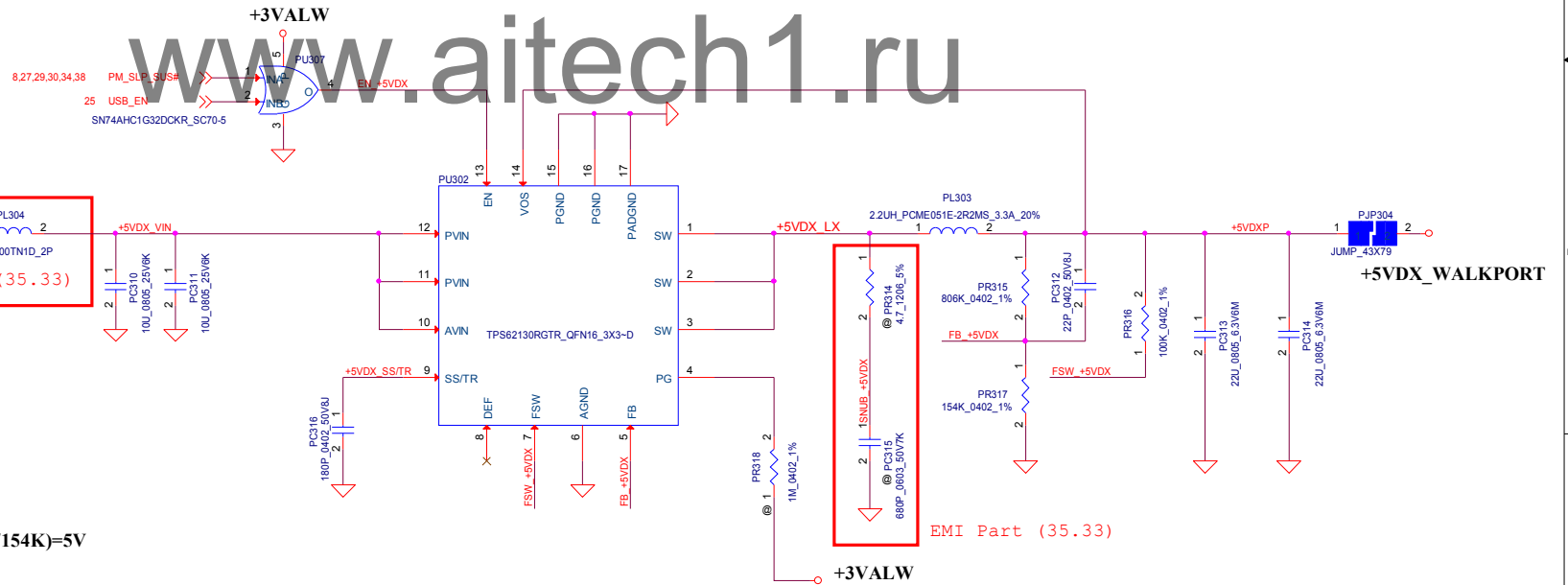
battery = 2S3P →
 2130mAh*3= 6390mAh
 →6390mAh*0.8C=5.112A for express charge
 Design charger current around 6A for worst case
 max discharge current setting @ 7.7A (around 1.2C)

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Size	Document Number	Rev		1.0	
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$$\langle V_o=5V \rangle \quad V_{FB}=0.8V$$

$$V_o=V_{FB} \cdot (1 + PR305/PR307) = 0.8 \cdot (1 + 806K/154K) = 5V$$



$$\langle V_o=5V \rangle \quad V_{FB}=0.8V$$

$$V_o=V_{FB} \cdot (1 + PR315/PR317) = 0.8 \cdot (1 + 806K/154K) = 5V$$

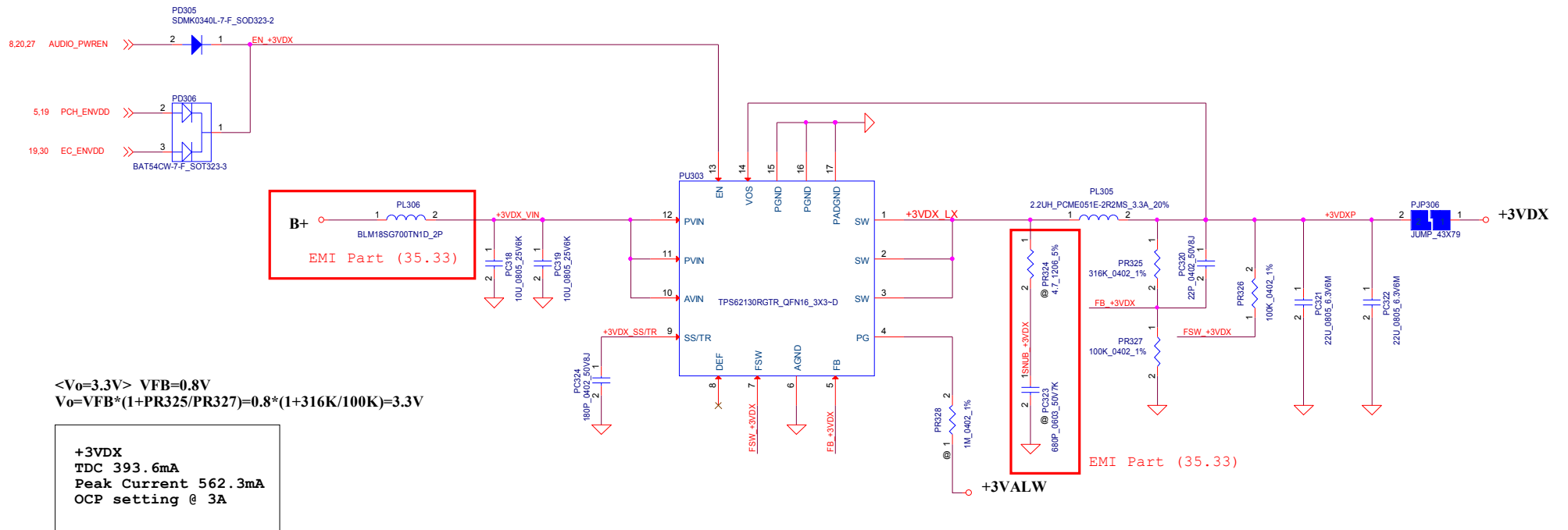
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				Deciphered Date				2013/10/28			
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								LA-9262P			
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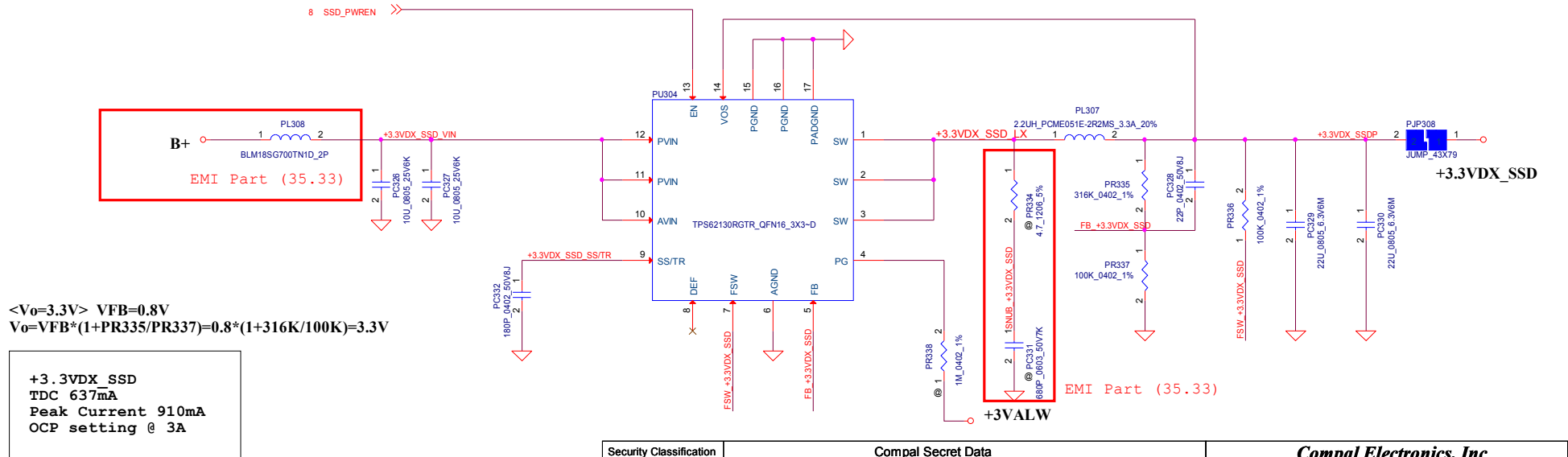
P32-PWR +5V_VR

LA-9262P

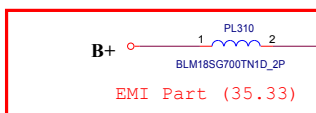
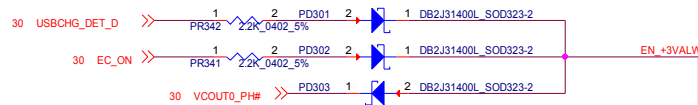
Rev 1.0



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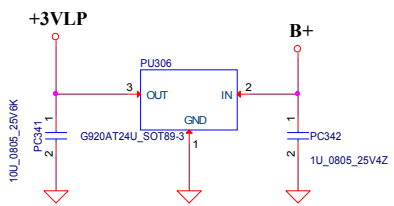
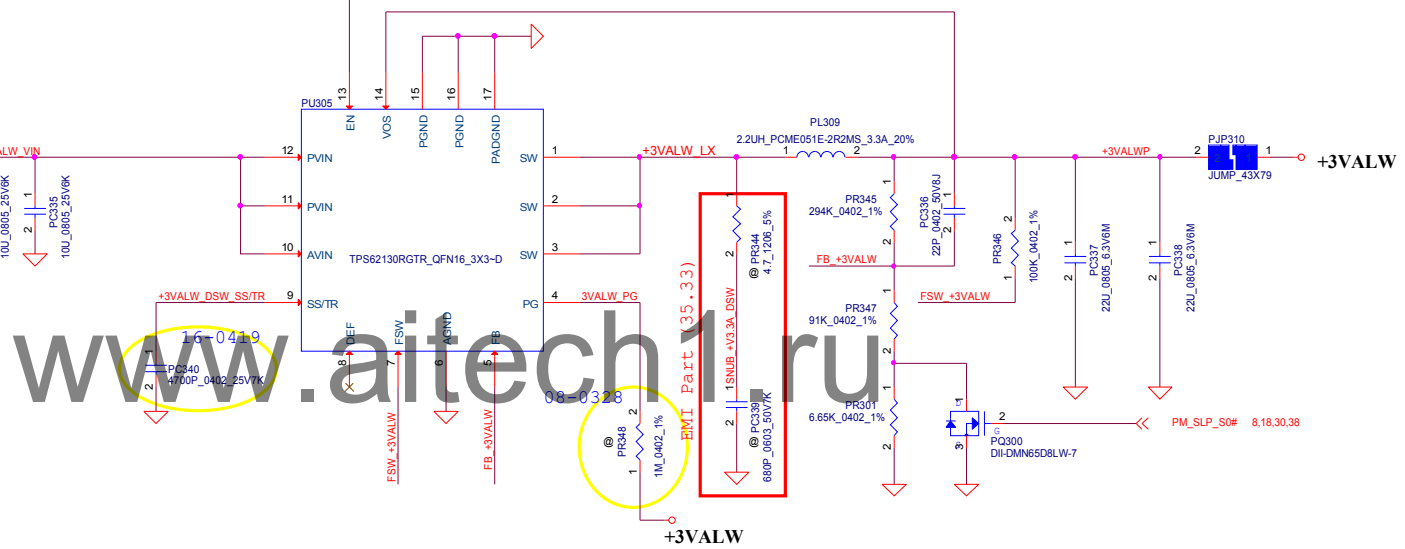


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						Size	Document Number			Rev	
						LA-9262P				1.0	
						Date:	Friday, April 19, 2013		Sheet	35	of

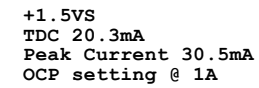


<V_o=3.3V> VFB=0.8V
 $V_o = V_{FB} * (1 + PR345/PR347) = 0.8 * (1 + 316K/100K) = 3.3V$

+3VALW
 TDC 161mA
 Peak Current 2301mA
 OCP setting @ 3A

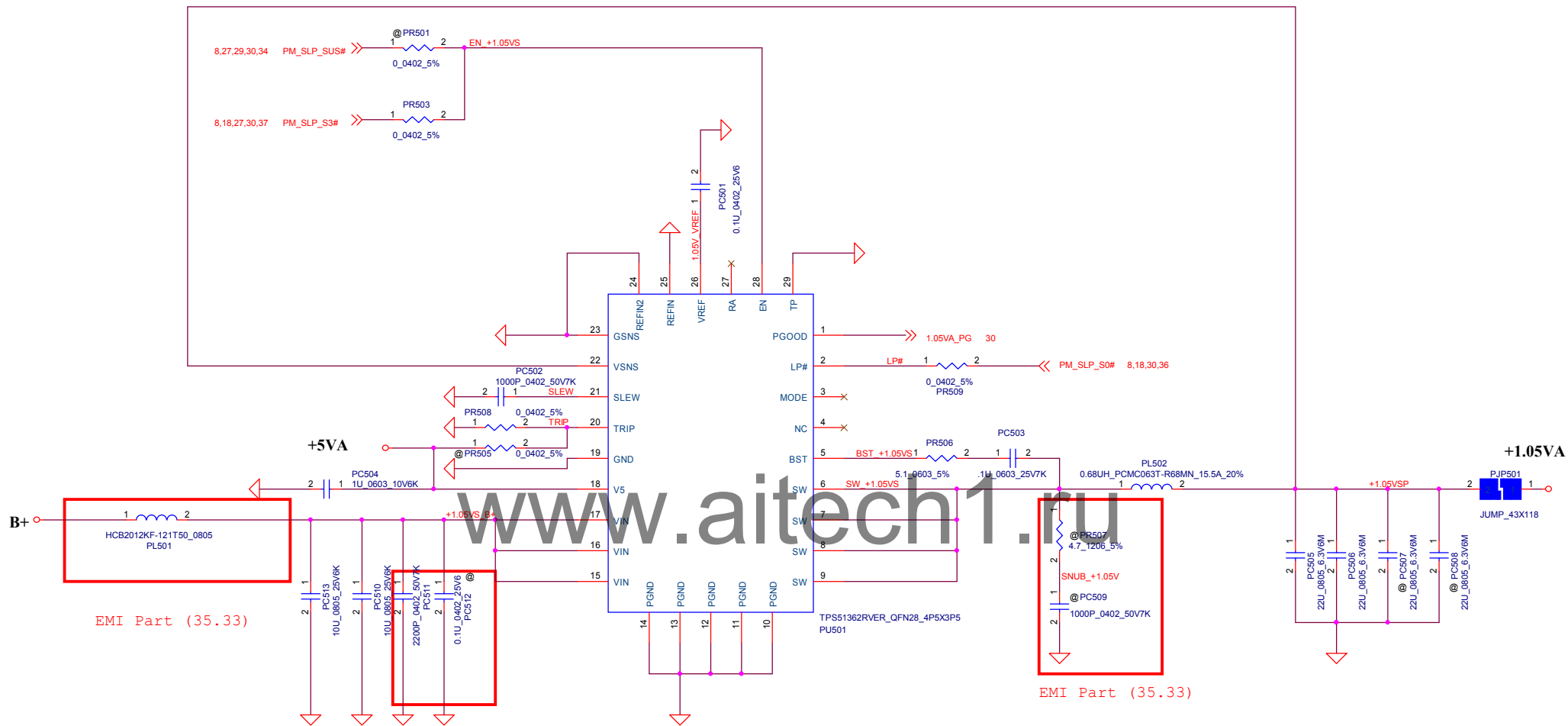


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Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	P34-PWR +3.3V VR(2/2)
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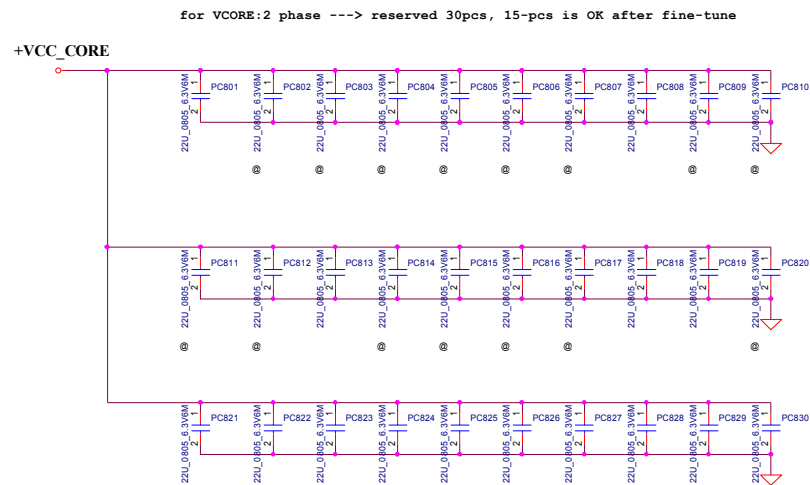


+1.8VS
TDC 11.9mA
Peak Current 17mA
OCP setting @ 2A

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				P39-PWR PROCESSOR DECOUPLING	
				Rev 1.0	
				Date: Friday, April 19, 2013	
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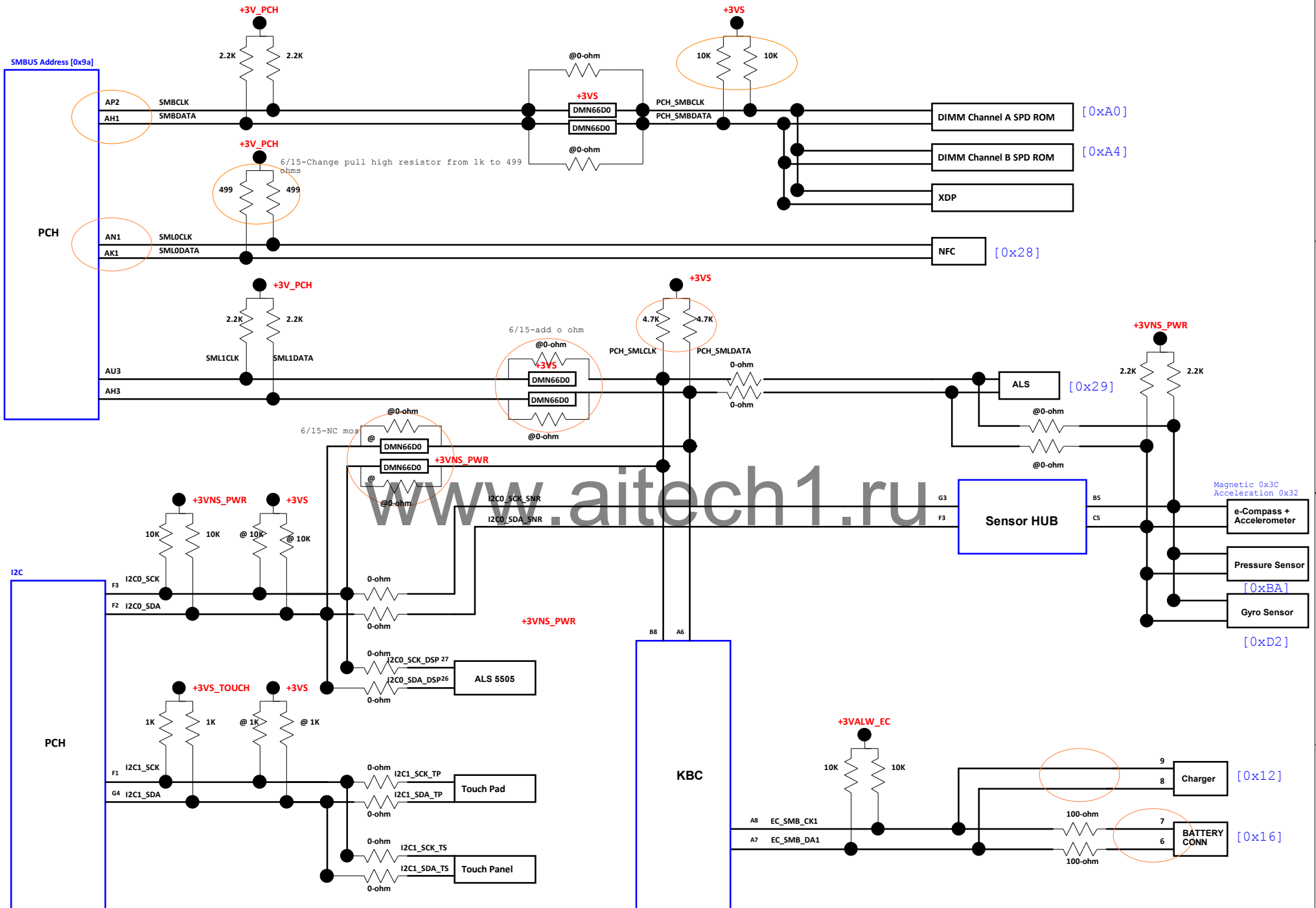
Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
X	XX	XXX	XX'XX/XX	Compal_XX	XXXXXX	Change PRXX from Xohm to XXKohm.	
36			20121008	Compal_Power	create one more input cap for TPS51362 Vin	add PC513_10U_0805_16V6K for TPS51362's input	
34			20121012	Compal_HW	create one more resistor for TPS62130 enable pin	add PR342_2.2K_0402_5%	
34			20121018	Compal_Power	design change, delete PU301-PU305, TPS62130 and related components, create PU301, TPS51225 for 3.3V and 5V power rails		
35							
36							
36			20121018	Compal_Power	design change, delete PU401, PU402, TPS62140 and TPS62150 and related components, create PU401and PU402, SY8003D for 1.5V and 1.8V power rails		
34			20121023	dell	reject power design change of 3.3V, 5V, 1.8V and 1.5V		
35							
36							
38			20121203	Compal_EMI	change PL501 for EMI and layout routing	change from SUPPRE_FBMA-L11-453215-800LMA90T_1812 to HCB2012KF-121T50_0805	
39			20121203	Compal_EMI	change PL601 for EMI and layout routing	change from SUPPRE_FBMA-L11-453215-800LMA90T_1812 to HCB2012KF-121T50_0805	
40			20121203	Compal_EMI	add PL703 for EMI	add PL701 HCB2012KF-121T50_0805	
38			20121203	Compal_Power	create PR509 0_0402_5% for debug	add PR509 0_0402_5%	
32			20121205	Compal_HW	create PR5107 10K_0402_1% for test	add PR107 10K_0402_1%	
40			20121213	Compal_Power	fine tune VR transient	de-pop PC714, change PR711 from 150K to be 100K	
40			20130122	Compal_Power	follow intel's recommendation	change PR737 from 110 OHM to be 130 OHM	
33			20130131	Compal_RF	reserved a MLCC for RF consideration	create PC206 2200P_0402_50V7K	
40			20130221	Compal_RF	for RF noise reducing	pop PC703, PR719 and PC712, PR734 and PC722 for VCORE	
39			20130221	Compal_RF	for RF noise reducing	pop PR605 and PC613 for DDR	

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